
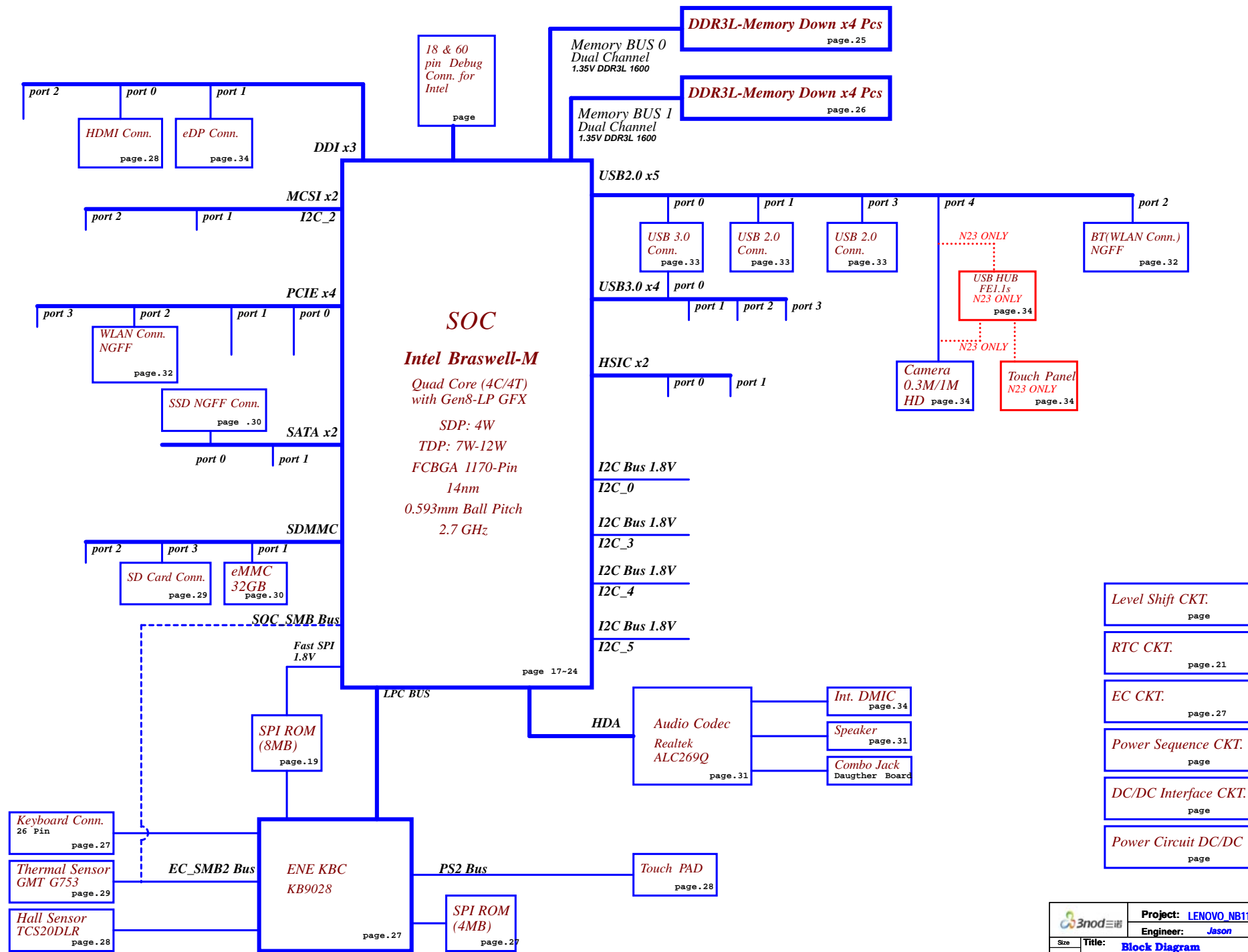


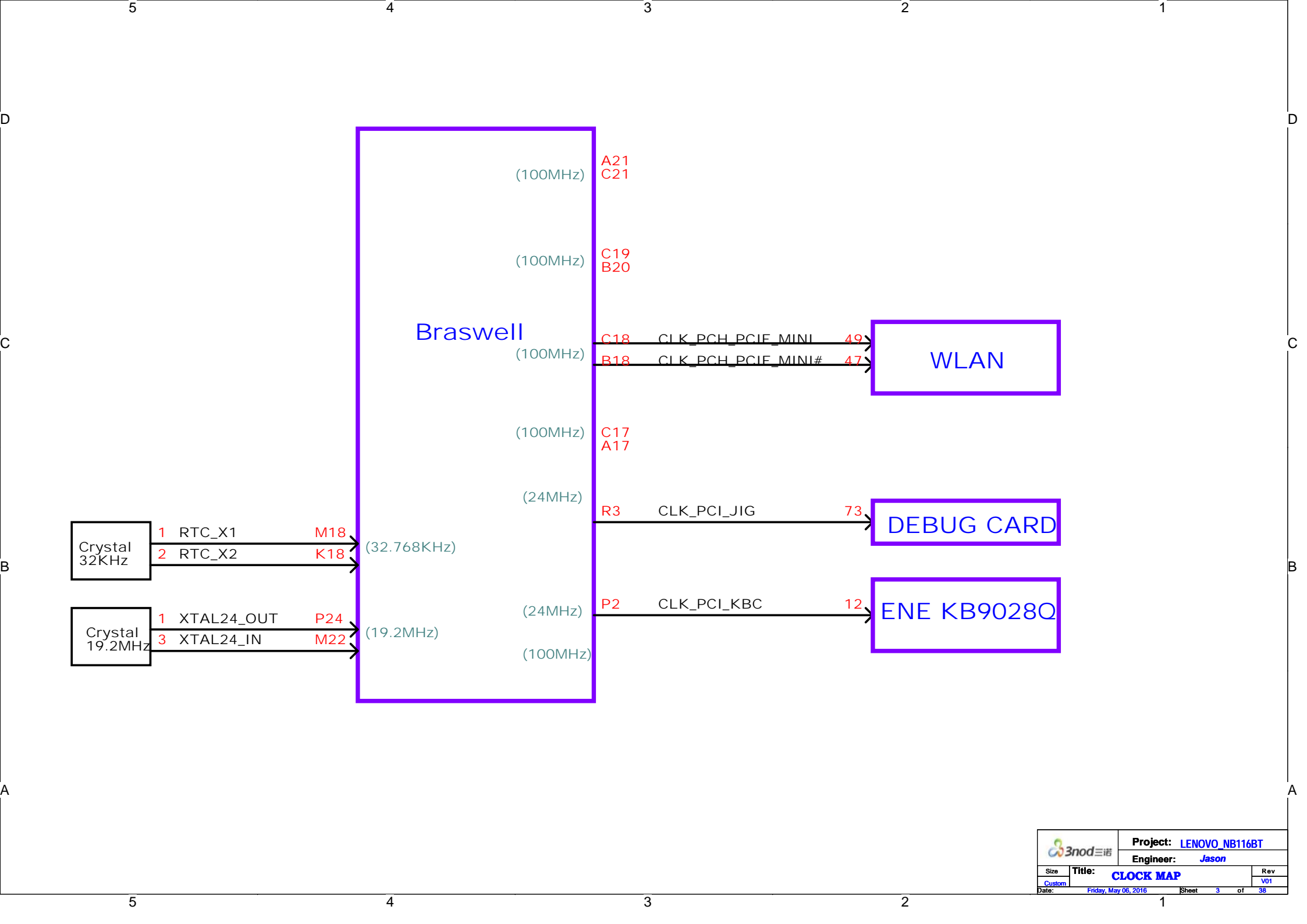
N23

01	--	COVER SHEET	21	--	BrasWell (LPC,RTC)
02	--	SYSTEM BLOCK DIAGRAM	22	--	BrasWell (USB,UART)
03	--	CLOCK MAP	23	--	Broadwell(POWER 1 OF 2)
04	--	POWER SEQUENCY DIAGRAM	24	--	BrasWell (POWER 2 OF 2)
05	--	POWER MAP	25	--	DDR3L (MD-1RX16)-A
06	--	SMBUS MAP	26	--	DDR3L (MD-1RX16)-B
07	--	DC Interface	27	--	EC+KBC (ENE9010) & ROM
08	--	PWR_DC CONN/BATT CONN	28	--	PWR LED/LID/TP CONN./HDMI
09	--	PWR_CHARGER	29	--	Micro SD CONN. & Thermal sensor
10	--	PWR_5V/3.3V	30	--	eMMC & M2 SSD
11	--	Empty	31	--	Audio (CODEC_ALC269Q)
12	--	PWR_DDR	32	--	WIFI & BT
13	--	PWR_VCC_CORE	33	--	USB3.0 & 2.0 CONN
14	--	PWR_VGG_CORE	34	--	eDP & CAM
15	--	PWR_MOIC	35	--	Sensor & HUB
16	--	Empty			
17	--	BrasWell (DISPLAY)			
18	--	BrasWell (DDR3L A/B)			
19	--	BrasWell (SPI,SATA,PCIE,AUDIO)			
20	--	BrasWell (GPIO/I2C/CLK)			

		Project: LENOVO_NB116BT	
		Engineer: Jason	
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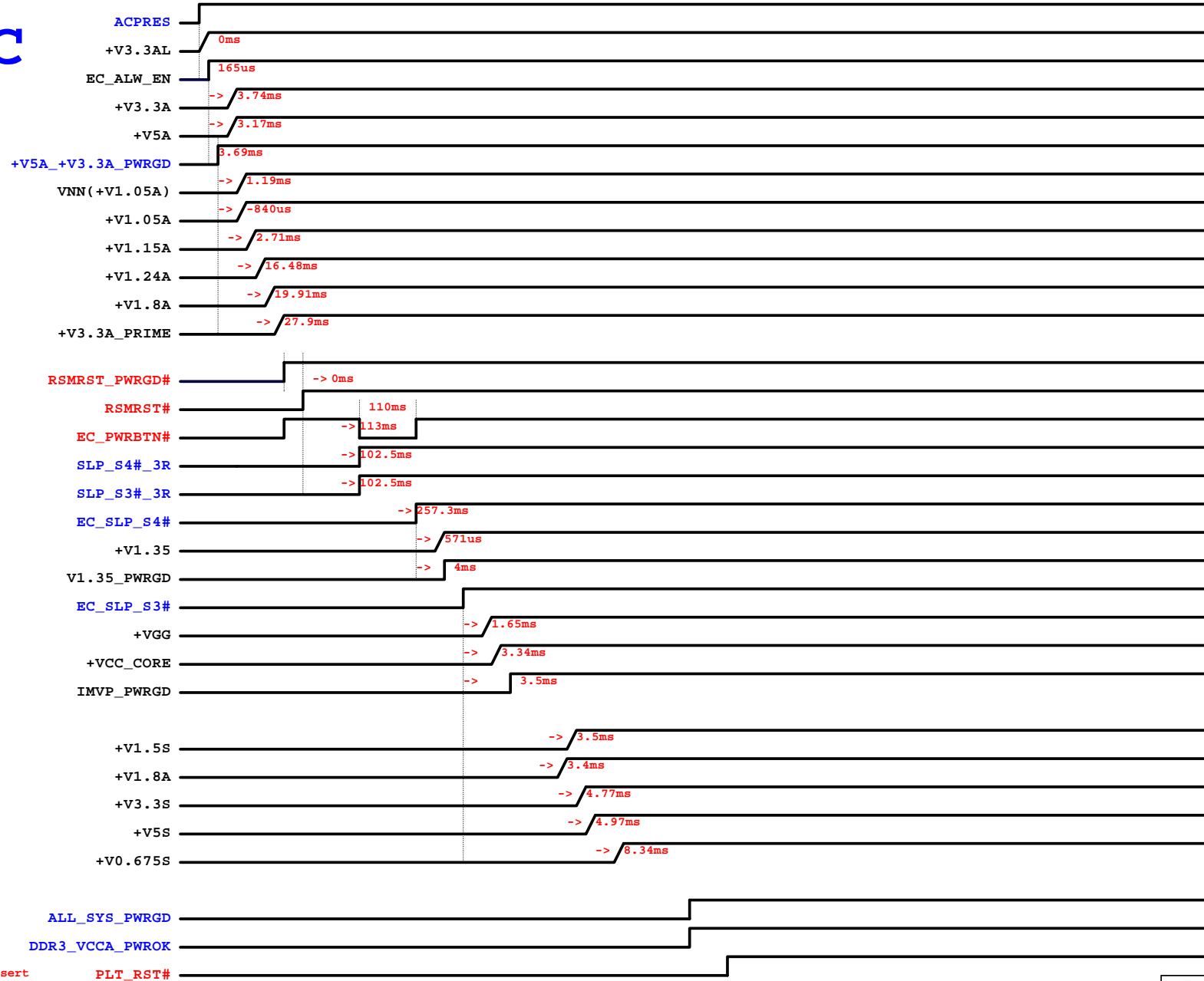
Block Diagram

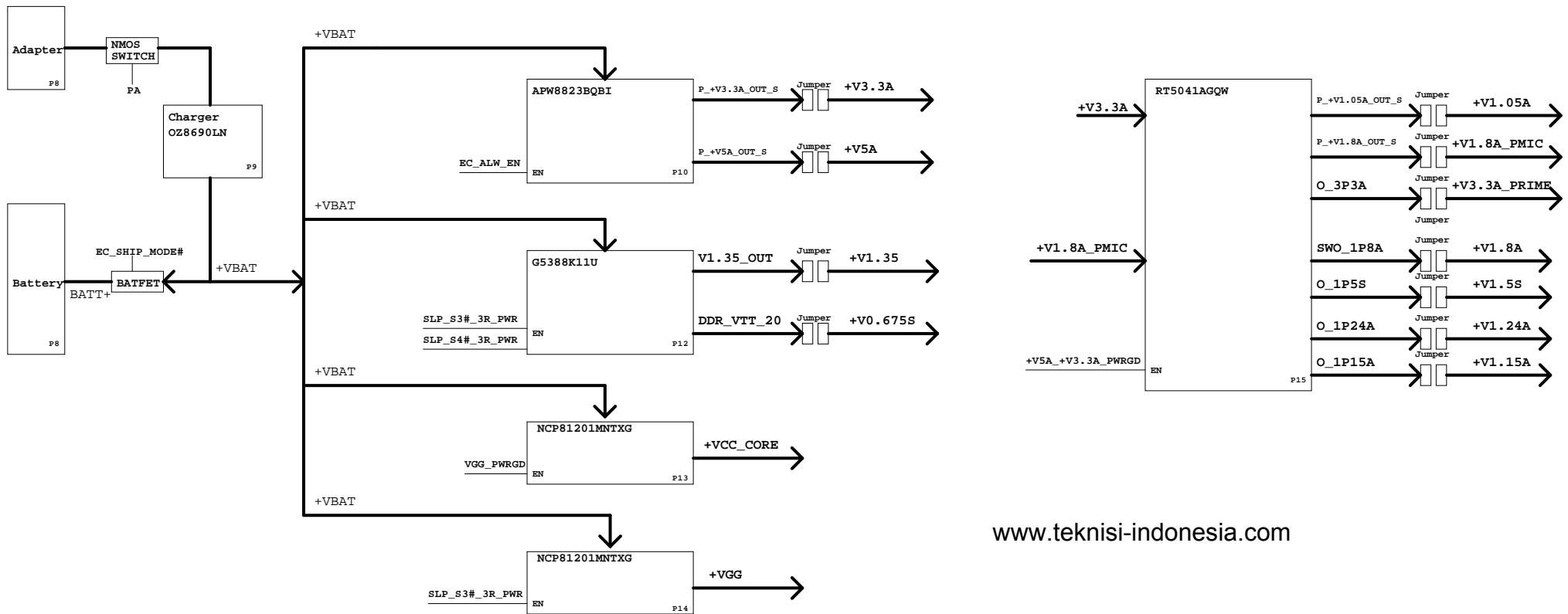




SOC

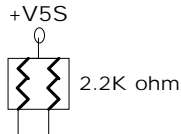
G3->S0



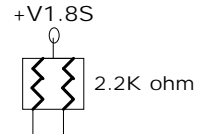
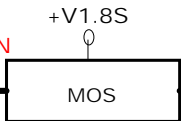


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HDMI



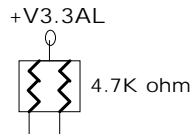
HDMI_DDC_DATA_IN_CON
HDMI_DDC_CLK_IN_CON



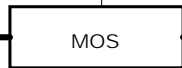
MHL_TMDS_DDC_DATA
MHL_TMDS_DDC_CLK



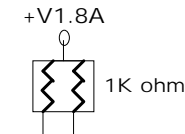
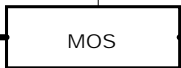
Braswell



+V3.3AL

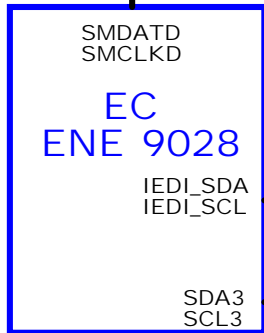
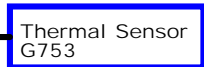


+V1.8A



TP_SMB_DAT_3A
TP_SMB_CLK_3A

TP_SMB_DAT_3S
TP_SMB_CLK_3S

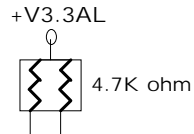


EC
ENE 9028

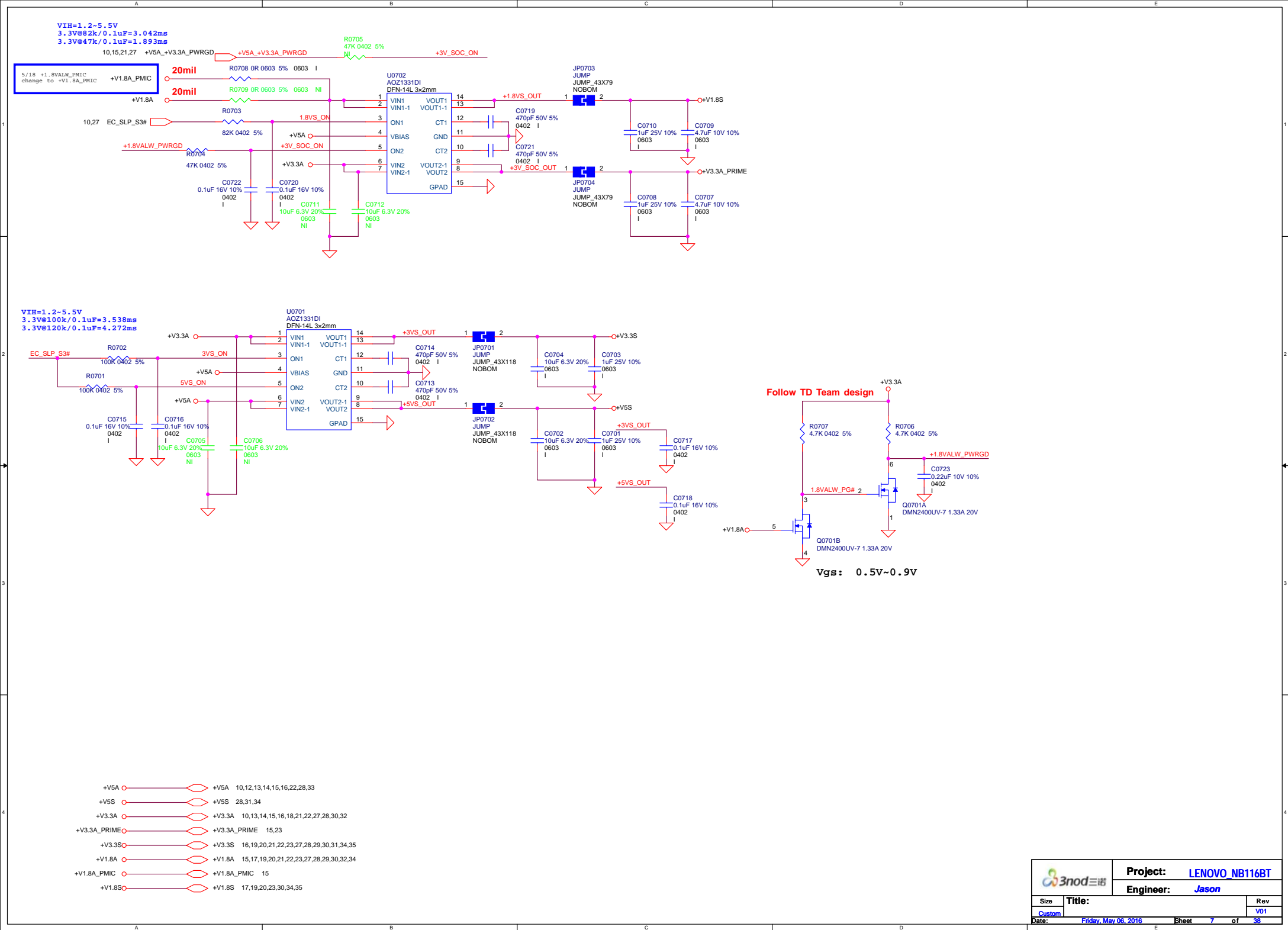
IEDI_SDA
IEDI_SCL

SDA3
SCL3

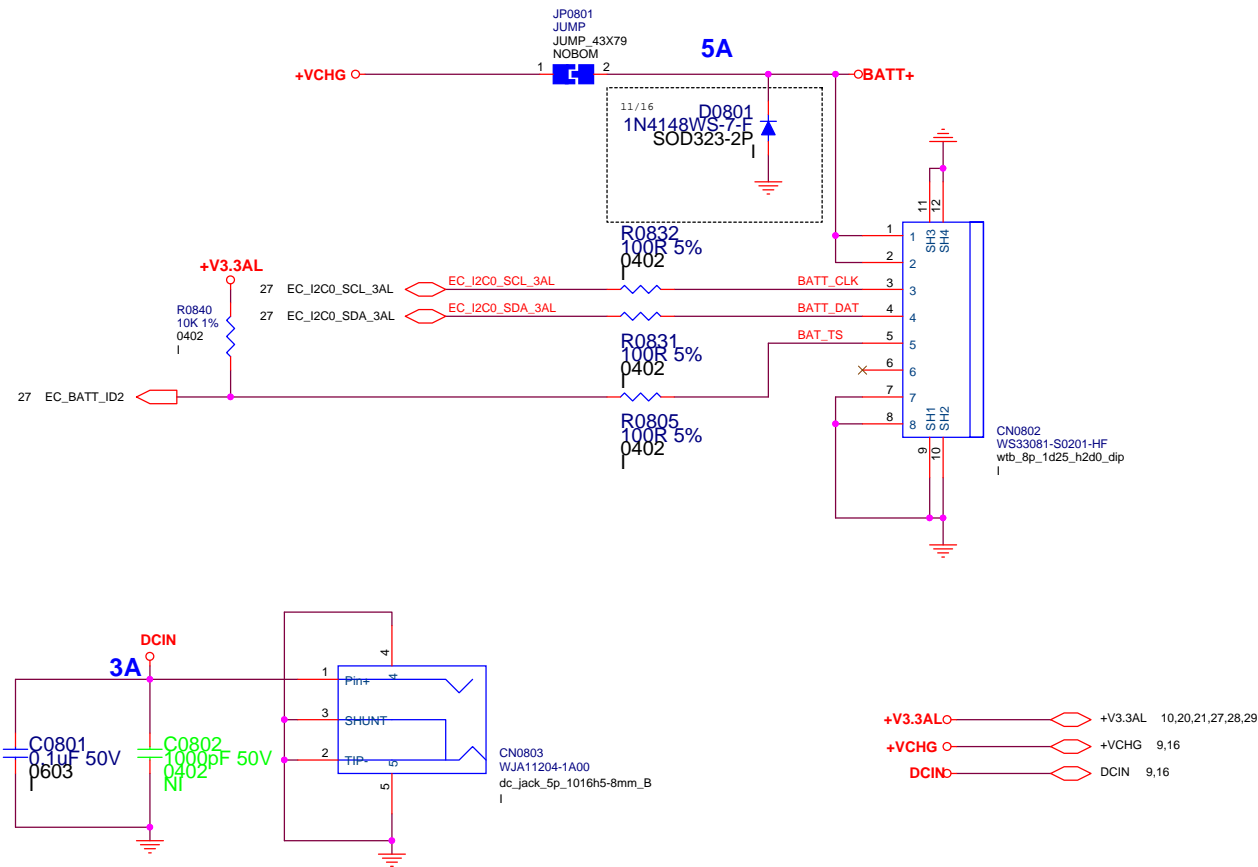
EC_SMB1_DAT_3AL
EC_SMB1_CLK_3AL



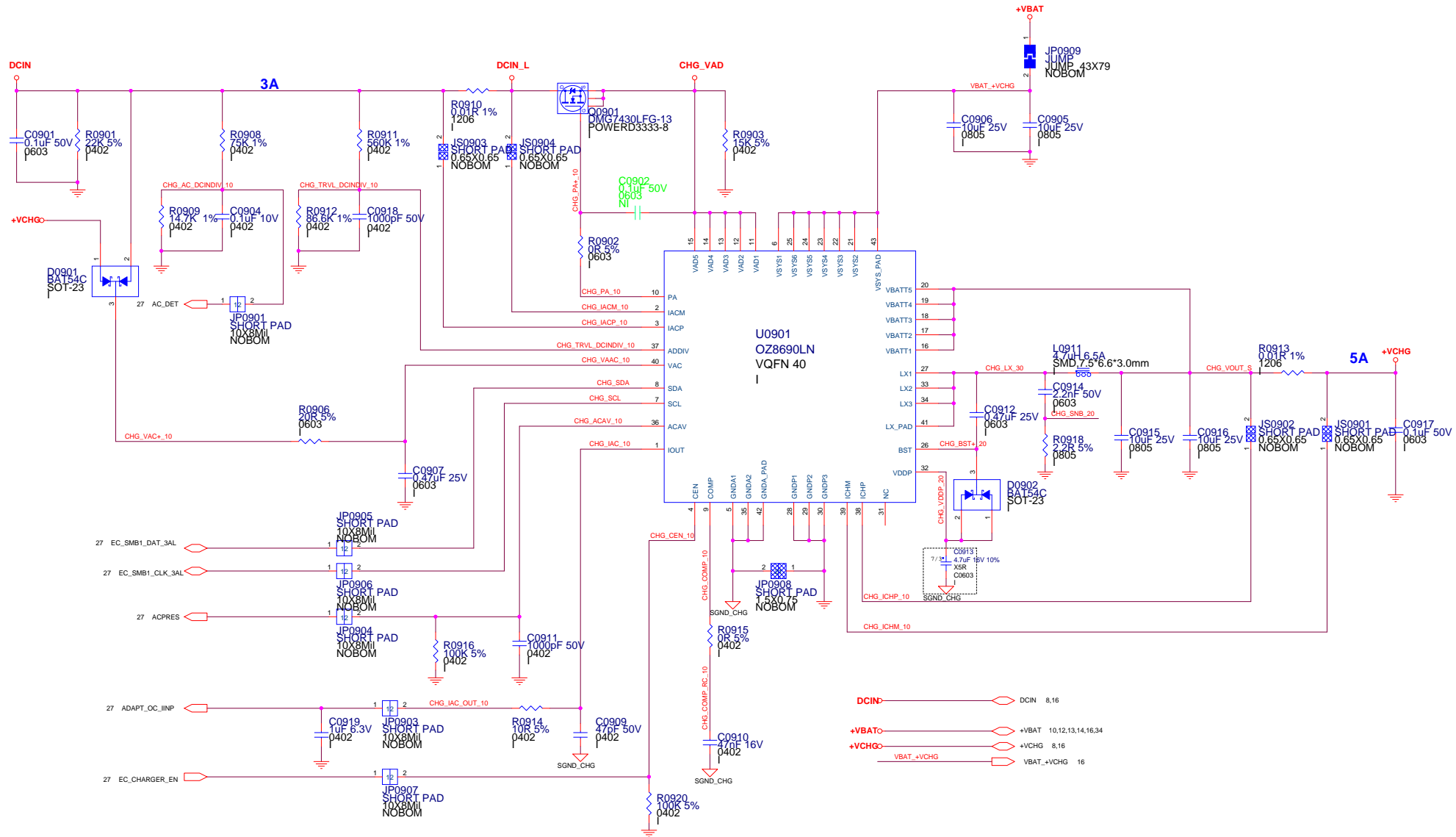
EC_I2C0_SDA_3AL
EC_I2C0_SCL_3AL



08: DC-IN & BATTERY CONNECTOR

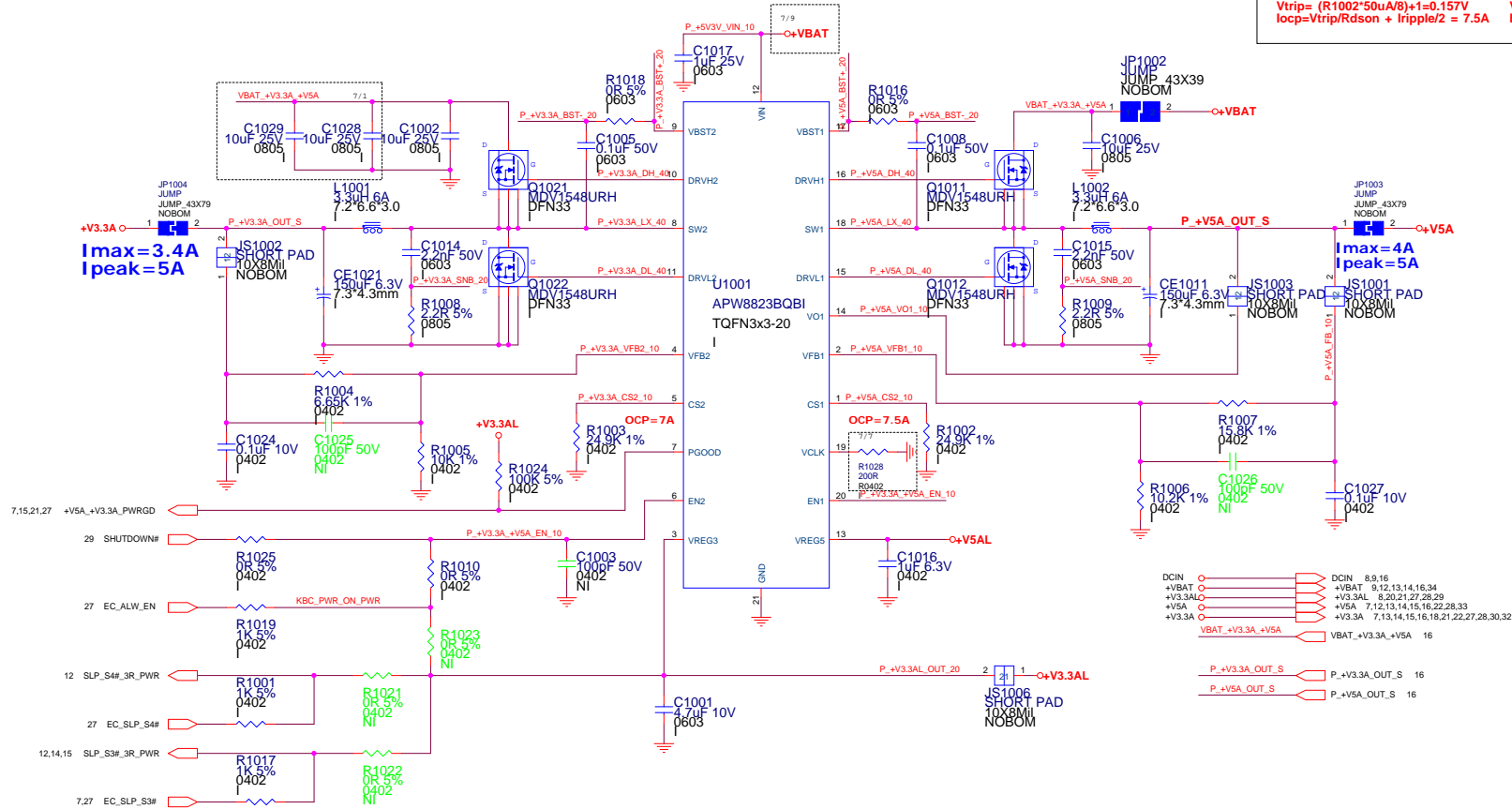


09: BATTERY CHARGER




10: +V5A / +V3.3A POWER SUPPLY

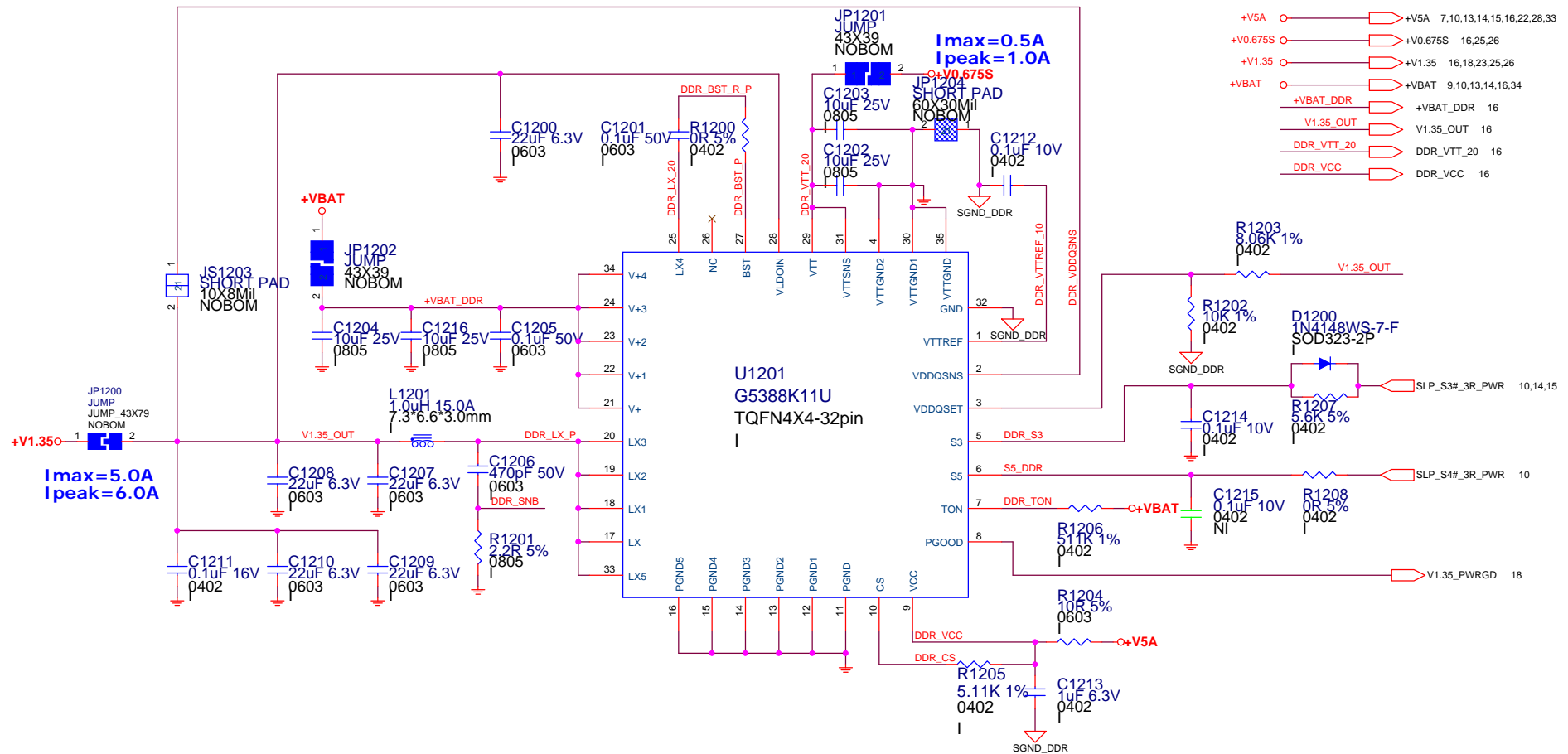
+V5A:	+V3.3A:
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.16A$	1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.22A$
2. Ripple Current: $I_{rip} = 3.72A$	2. Ripple Current: $I_{rip} = 2.36A$
3. Ripple Voltage: $ESR/1 = 15m\Omega$ $V_{rip} = 55.8mV$	3. Ripple Voltage: $ESR/1 = 15m\Omega$ $V_{rip} = 35.4mV$
4. Inductor Spec: $I_{sat} = 9.3A$ $I_{dc} = 6.3A$ $DCR = 30m\Omega$	4. Inductor Spec: $I_{sat} = 9.3A$ $I_{dc} = 6.3A$ $DCR = 30m\Omega$
5. MOSFET Spec: H/L-side MOSFET: MDV1548URH $R_{ds(ON)} = 27.8m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 8.6A$ ($T = 25^\circ C$)	5. MOSFET Spec: H/L-side MOSFET: MDV1548URH $R_{ds(ON)} = 27.8m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 8.6A$ ($T = 25^\circ C$)
6. Frequency: $F = 400KHz$	6. Frequency: $F = 475KHz$
7. OCP: Set = R1002 to 24.9K $V_{trip} = (R1002 \cdot 50uA/8) + 1 = 0.157V$ $I_{ocp} = V_{trip} / R_{ds(on)} + I_{ripple}/2 = 7.5A$	7. OCP: Set = R1003 to 24.9K $V_{trip} = (R1003 \cdot 50uA/8) + 1 = 0.157V$ $I_{ocp} = V_{trip} / R_{ds(on)} + I_{ripple}/2 = 7.0A$



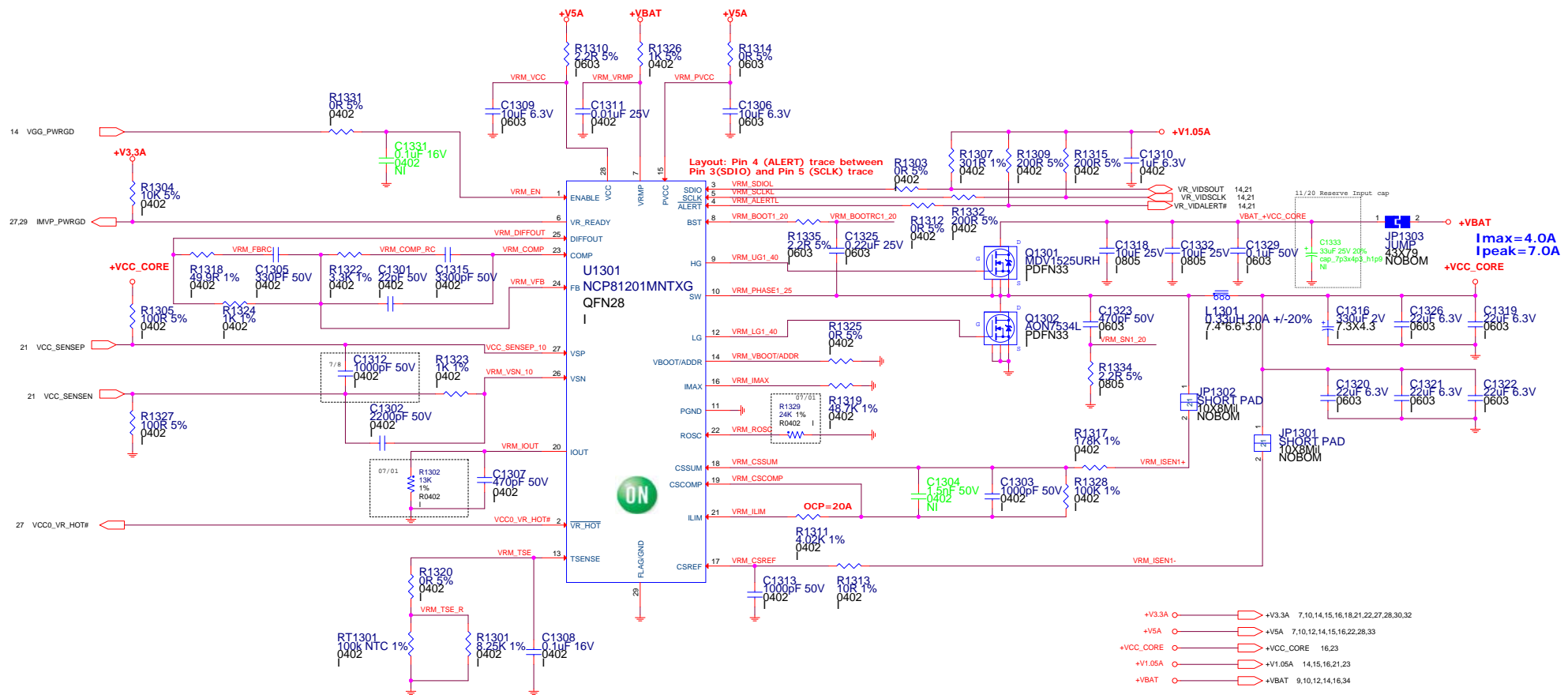
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		Project: LENOVO_NB116BT	
		Engineer: Jason	
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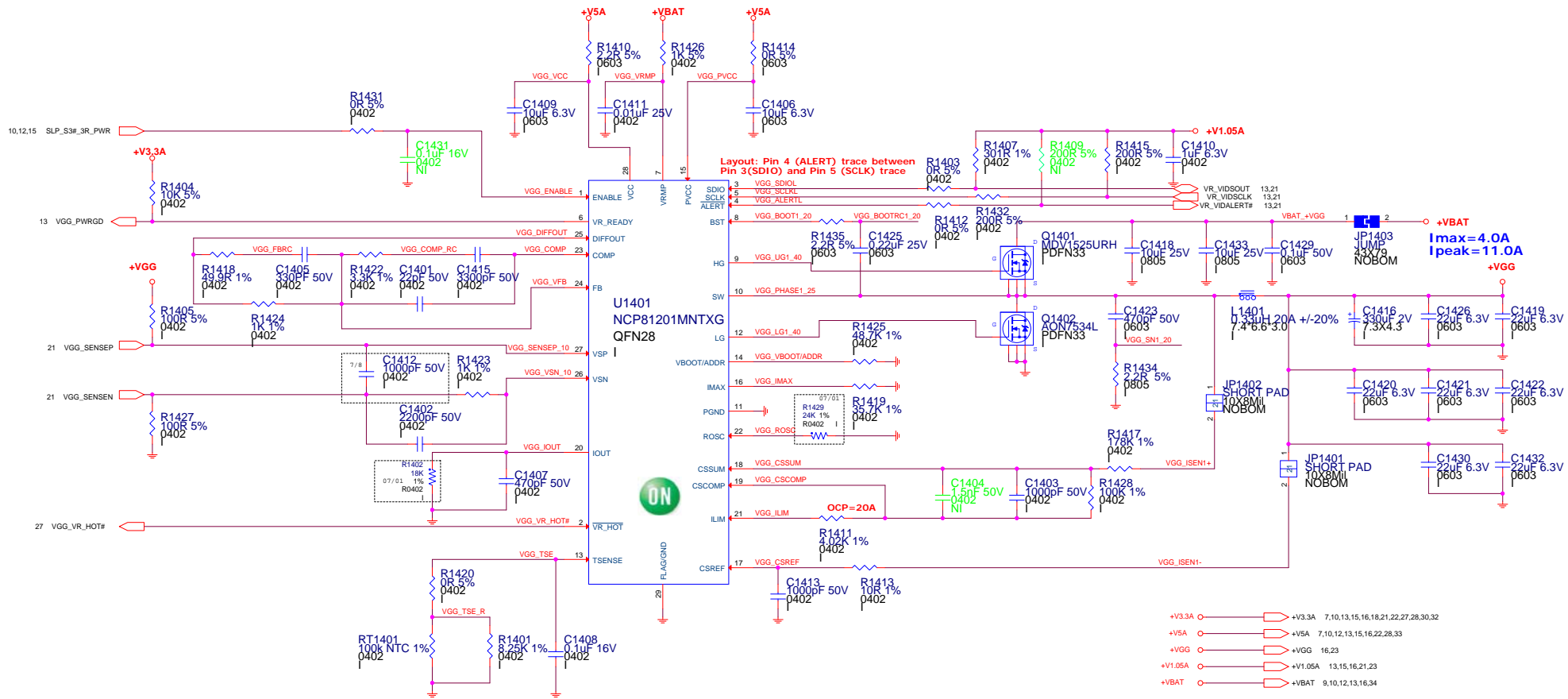
12: DDR POWER SUPPLY



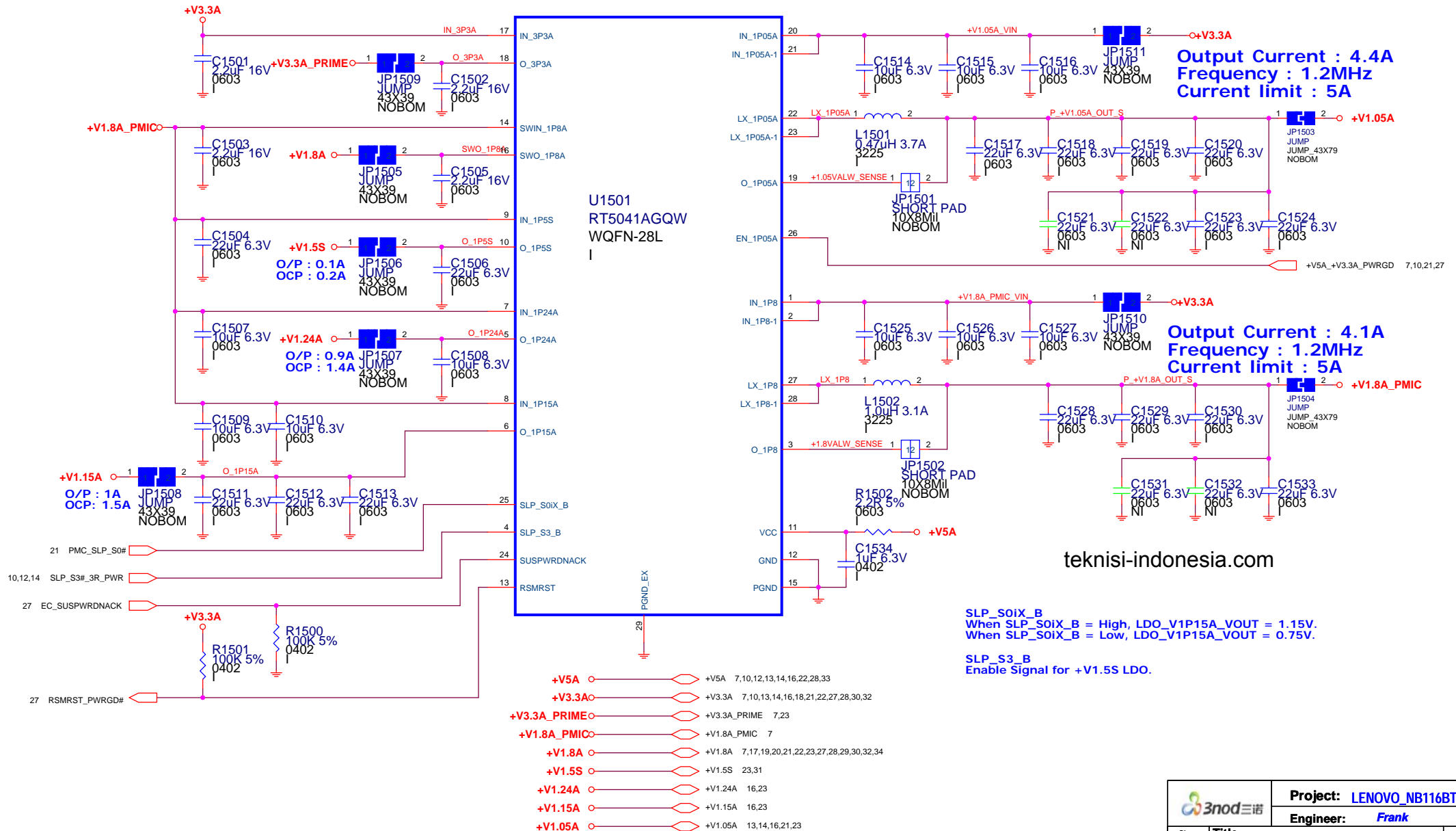
13: VCC0&VCC1 VCore POWER SUPPLY



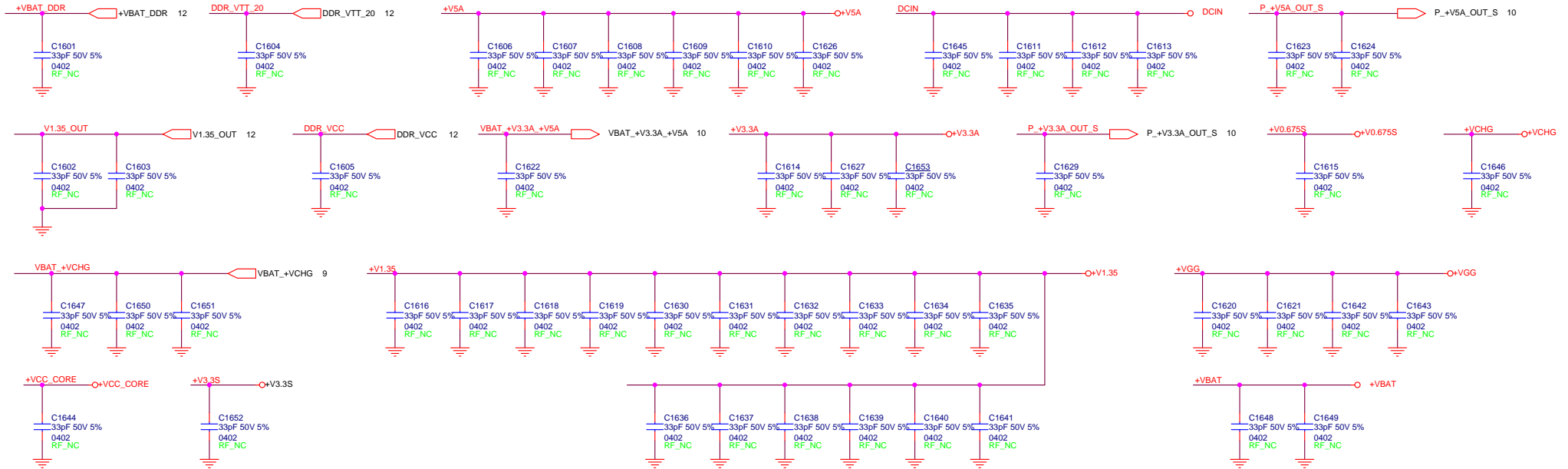
14: +VGG POWER SUPPLY



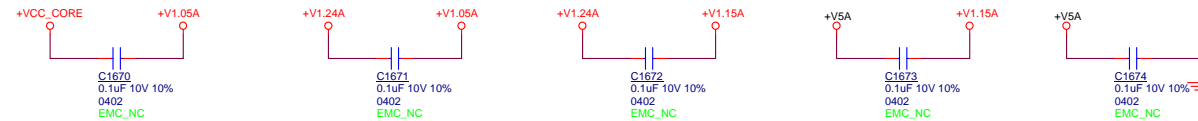
15: MOIC POWER SUPPLY



16 : RF Solution

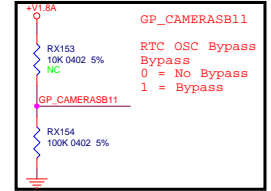
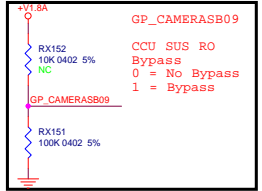
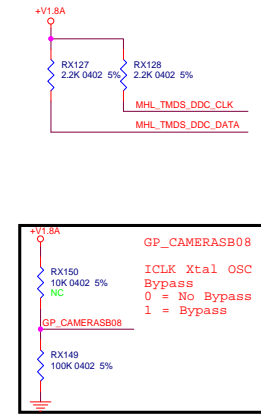
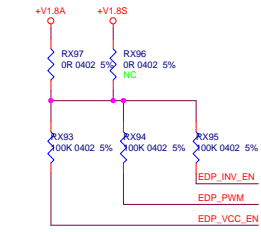
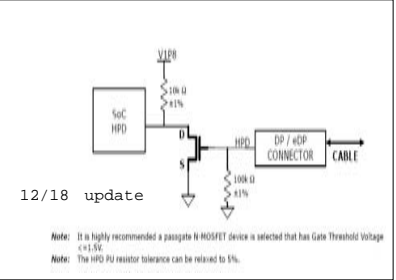


EMC Solution



3.4.4 DDI Disable Guidelines

Pin Name	System Pull-up/ Pull-down	Schematics Notes	✓
DDIx_TXP[3:0] DDIx_TXN[3:0]		No Connect	
DDIx_AUXP DDIx_AUXN		No Connect	
DDIx_HPD DDIx_DDC_CLK DDIx_DDC_DATA		No Connect	
DDIx_BKLTEN DDIx_BKLTCTL DDIx_VDDEN		No Connect	
DDIx_RCOMP_P DDIx_RCOMP_N		402 Ω ±1%	



3.6 Storage Interfaces

3.6.1 SD Card Interface

Secure Digital Card (SD Card). If µSD is not implemented, leave them NC except RCOMP.

ESD and EMI components must be placed on board.

Pin Name	System Pull-up/ Pull-down	Series Termination	Notes	✓
SDMMC3_D[3:0]	N/A	10 Ω	Bi-directional port used to transfer data to and from SD/HMC card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].	

3.5.1 MIPI*-CSI-2 Interface—Four (x4) Lanes

If MIPI*-CSI-1 are not implemented, leave them NC.

Pin Name	System Pull-up/ Pull-down	Notes	✓
MCSI_1_CLKP MCSI_1_CLKN	N/A	Point to Point connection to rear camera.	
MCSI_1_DP[3:0] MCSI_1_DN[3:0]	N/A	Point to Point connection to rear camera.	

Pin Name	System Pull-up/ Pull-down	Notes	✓
MCSI_2_CLKP MCSI_2_CLKN	N/A	Point to Point connection to front camera.	

3.5.2 Other MIPI*-CSI and Compensation Interface

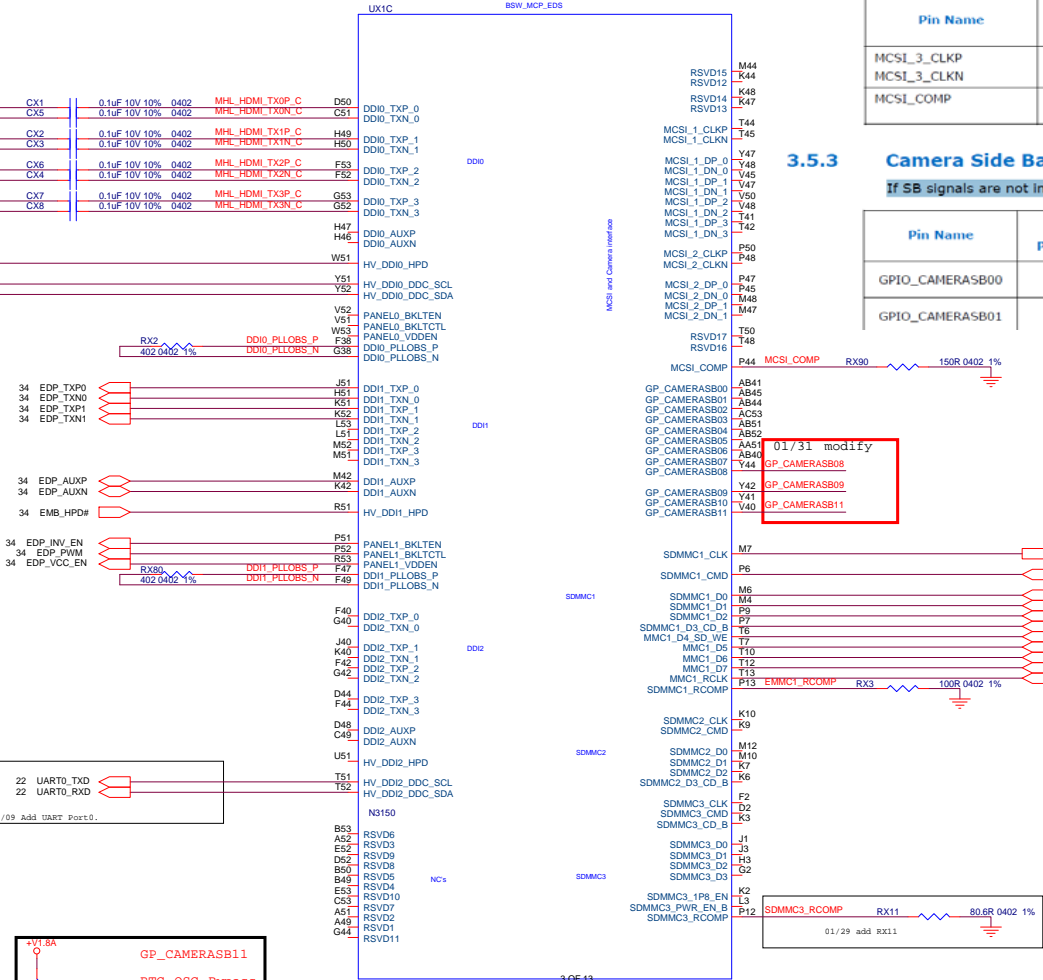
If the other MIPI*-CSI signals (exclude MCSI_COMP) are not implemented, leave them NC.

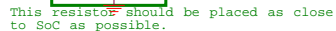
Pin Name	System Pull-up/ Pull-down	Notes	✓
MCSI_3_CLKP MCSI_3_CLKN	N/A	Point to Point connection to front camera.	
MCSI_COMP	150 Ω (±1%) PD to GND.	This resistor should be placed as close to SoC as possible.	

3.5.3 Camera Side Band Signals

If SB signals are not implemented, leave them NC.


Pin Name	System Pull-up/ Pull-down	Notes (as example in CRB)	✓
GPIO_CAMERASB0		Connect from SoC to CAM_ACT_LED to control camera privacy LED.	
GPIO_CAMERASB1		Connect from SoC to FLASH_RESET_N at camera module.	





21_27 ALL_SYS_PWRGD RX171 1K 5% | G1



	Project: LENOVO NB116BT		
	Engineer: Jason		
	Title: BrasWell (DDR3L A/B)		
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PCI-E Port Table

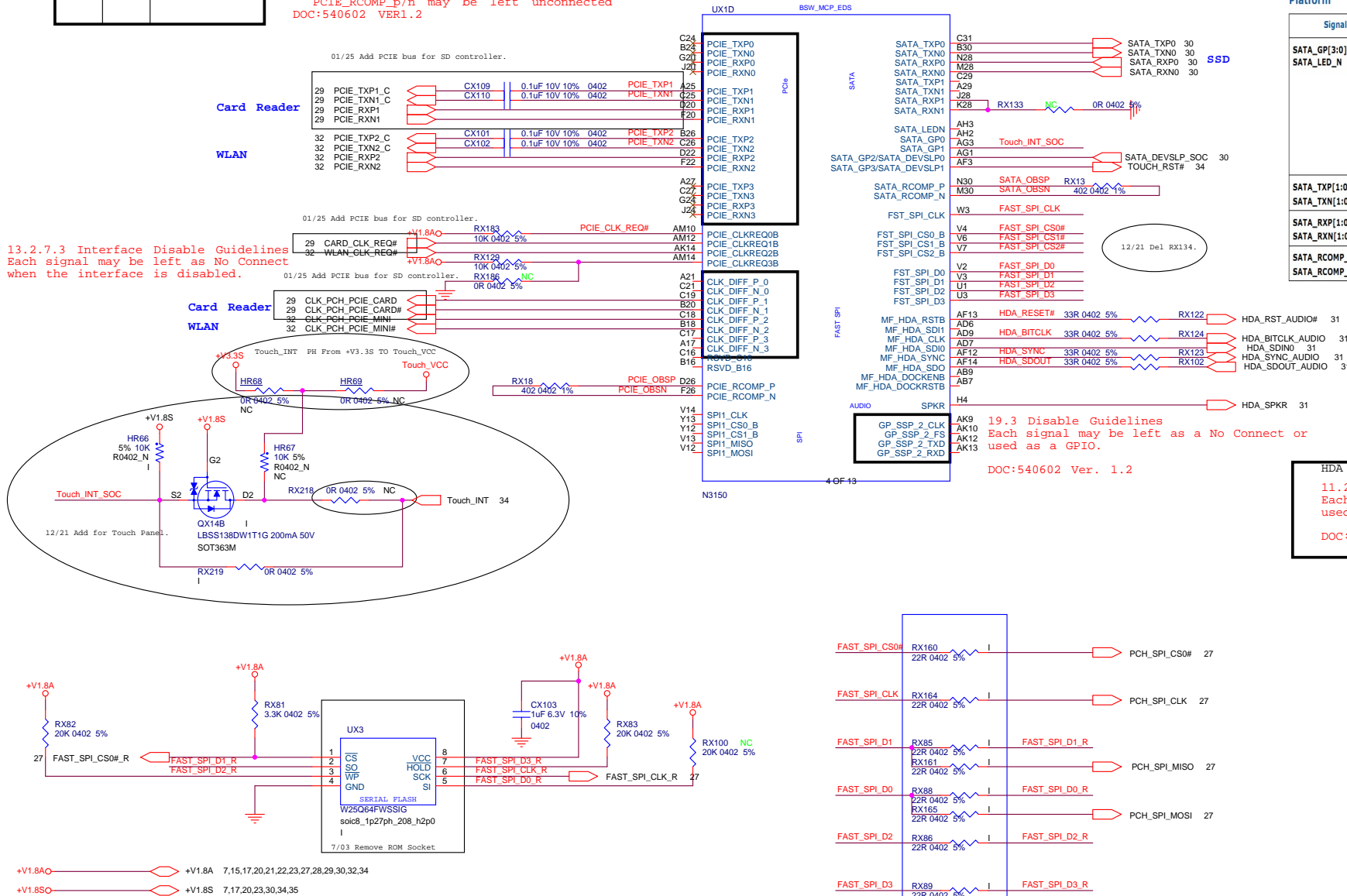
Port	CLK	Function
Port0	Port0	Un-used
Port1	Port1	WLAN (M.2)
Port2	Port2	Un-used
Port3	Port3	WLAN (MINI)

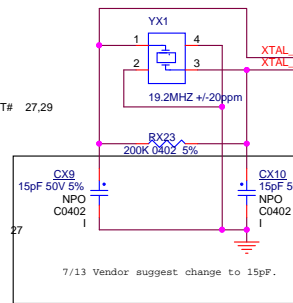
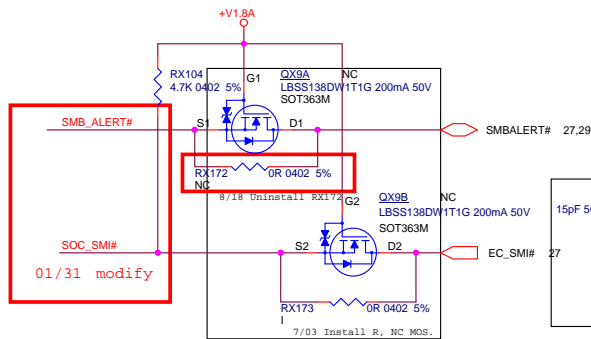
7.2.2 Terminating Unused PCI Express* Ports
 If some of the PCI Express* port(s) is not implemented on the platform:
 PCIE_TXP/N [x] and PCIE_RXP/N [x] signals may be left unconnected, where
 - x is the port number left no connect.
 If no PCI Express* ports is implemented on the platform:
 PCIE_TXP/n [3:0] and PCIE_RXp/n [3:0] may be left unconnected.
 Pull-up PCIE_CLKREQ[3:0]_N to V1P8A with 10-K? resistor.
 PCIE_RCOMP_p/n may be left unconnected
 DOC:540602 Ver1.2

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Table 9-7. Disable Guideline--If the Whole SATA interface are not Implemented on the Platform

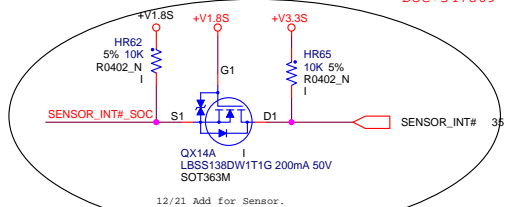
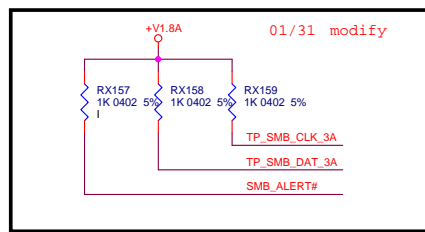
Signal Name	Disable Guideline
SATA_GP[3:0] SATA_LED_N	Each signal may be left as a No Connect or used as a GPIO. Additional considerations for each option are listed below. <ul style="list-style-type: none"> No Connect: Disable the relevant interface controller via the corresponding Soft Strap listed in the Braswell SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPO by means of the system BIOS. See the BIOS Writers Guide for further details. GPIO: Disable the relevant interface controller via the corresponding Soft Strap listed in the Braswell SoC Family SPI Flash Programming Guide. Additionally, configure the ball to be a GPI or GPO by means of the system BIOS. See the BIOS Writers Guide for further details.
SATA_TXP[1:0] SATA_TXN[1:0]	No-Connect.
SATA_RXP[1:0] SATA_RXN[1:0]	Connect to Ground.
SATA_RCOMP_P SATA_RCOMP_N	Connect as defined in Section 9.2.3, "SATA_RCOMP Compensation Guidelines".



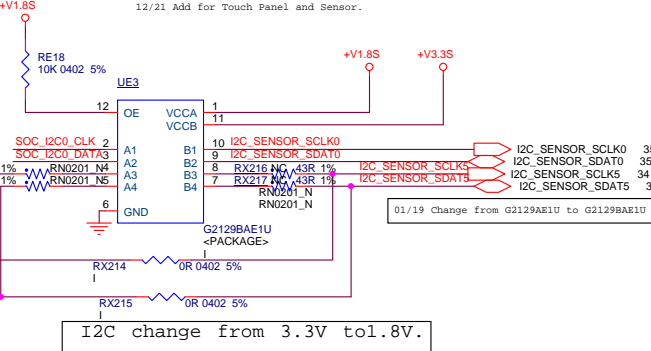
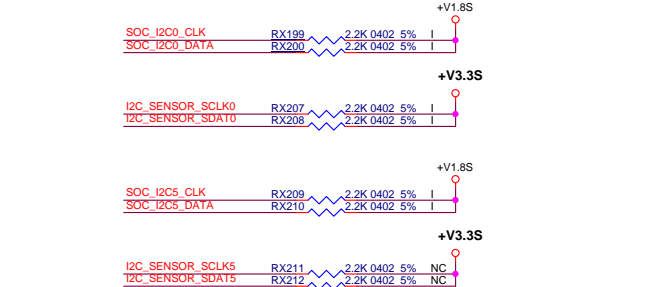
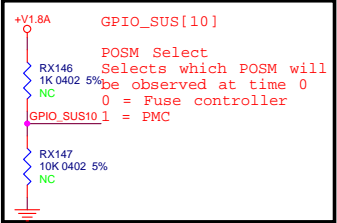
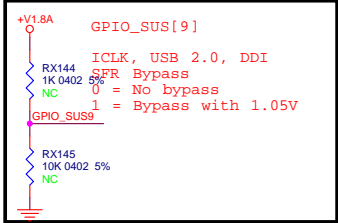
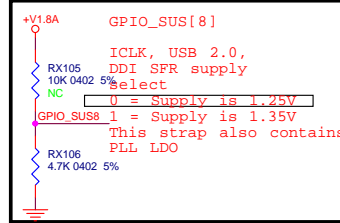
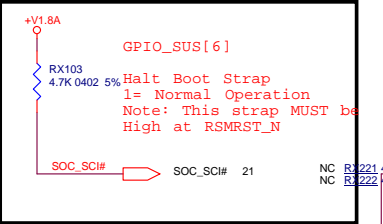
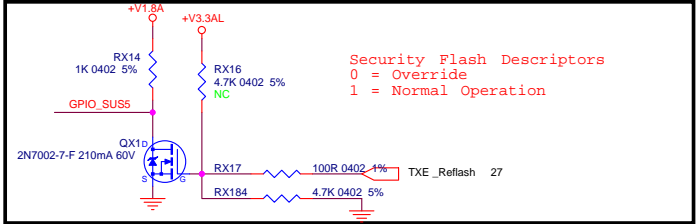
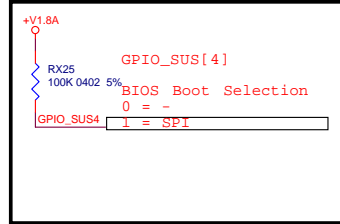
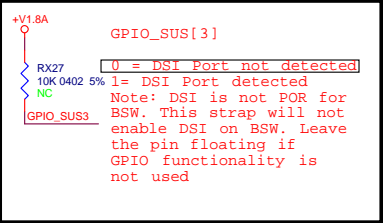
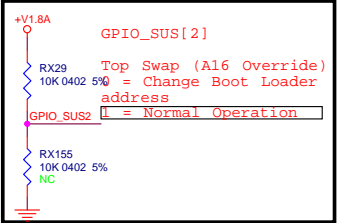
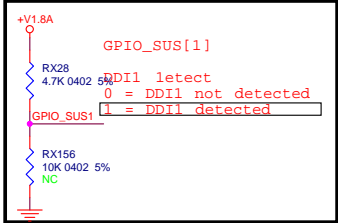
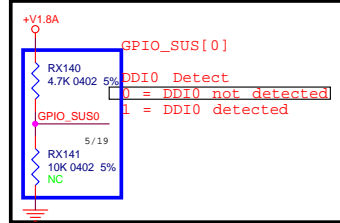
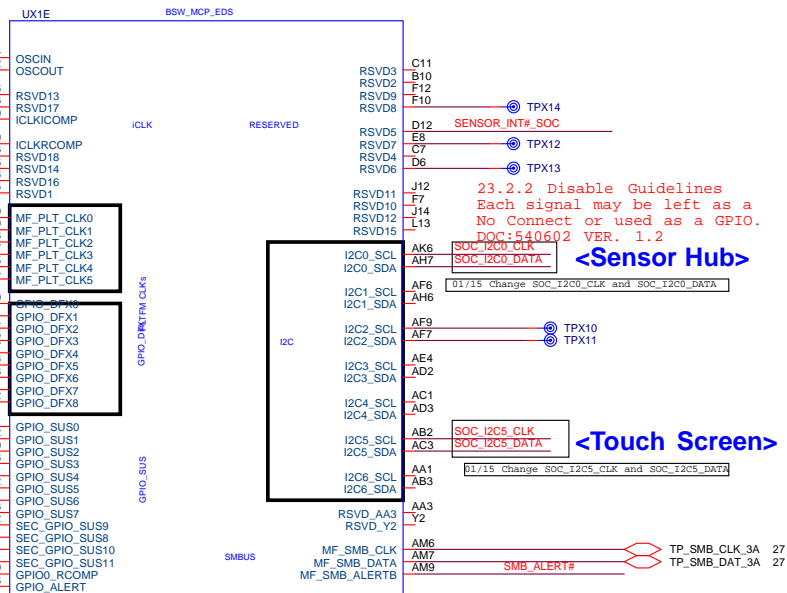


13.2.7.3 Interface Disable Guidelines
 Each signal may be left as No Connect when the interface is disabled
 DOC:540602 Ver. 1.2

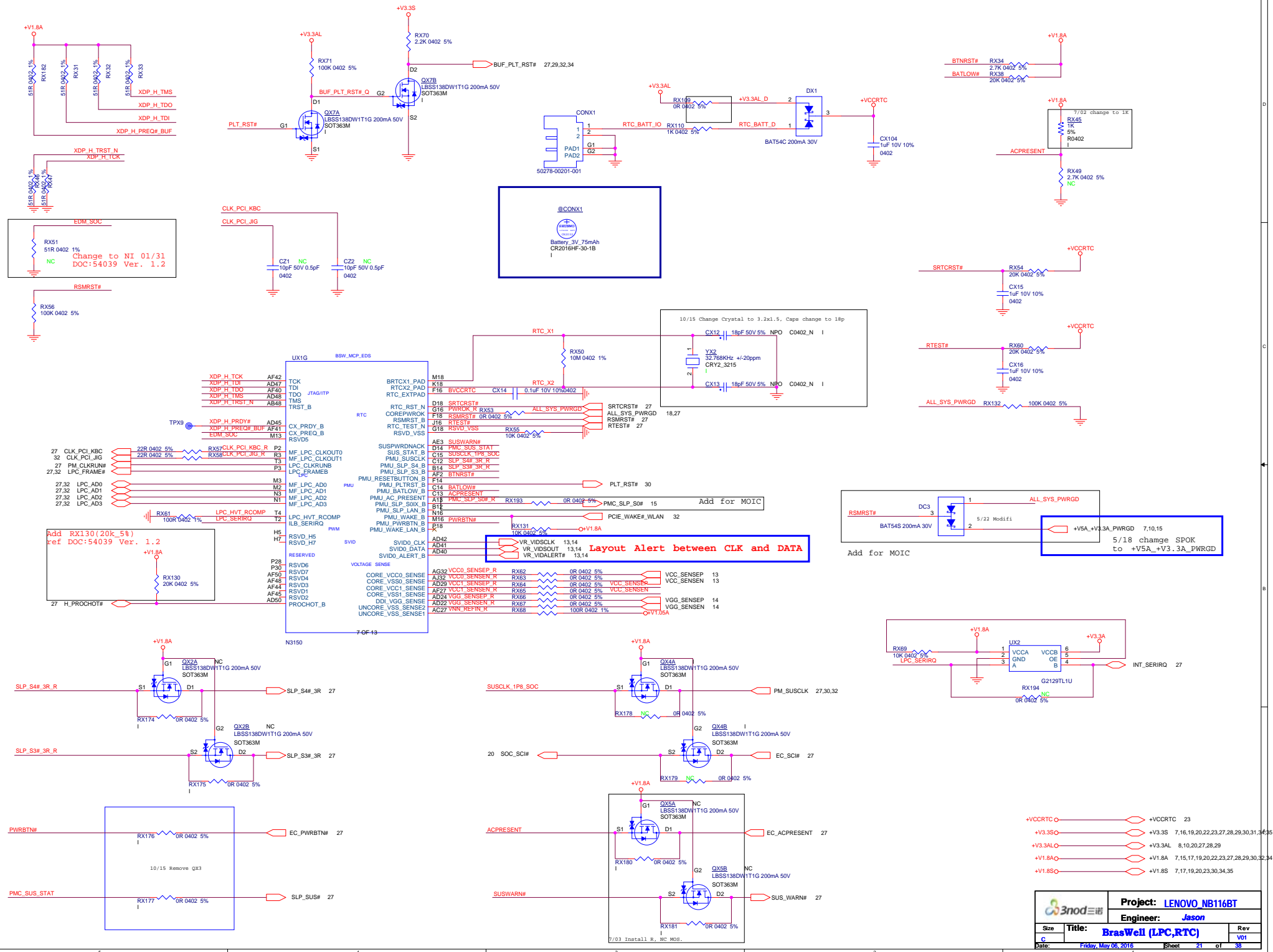
2.5 GPIO Multiplexing
 Note: Default Function for GPIO_DFX[8:0] is listed as RSVD but they can be used for normal GPIO functionality.
 DOC:547869 Rev. 1.2v1



- GPIO_SUS0
- GPIO_SUS1
- GPIO_SUS2
- GPIO_SUS3
- GPIO_SUS4
- GPIO_SUS5
- SOC_SCI#
- SOC_SMI#
- GPIO_SUS9
- GPIO_SUS8
- GPIO_SUS10
- GPIO_RCOMP18



- +V1.8A
- +V3.3A



*Need setting by BIOS

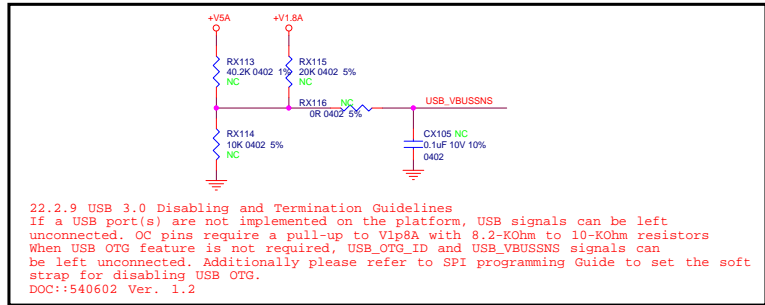
USB 3.0	USB 2.0	Function	OC#
PORT-0	PORT-0	USB2.0/3.0	OC#0
	PORT-1	USB2.0	OC#1
	PORT-2	BT	
	PORT-3	USB2.0	OC#1
	PORT-4	Webcam	

USB3.0

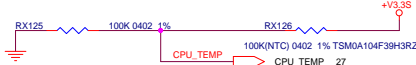
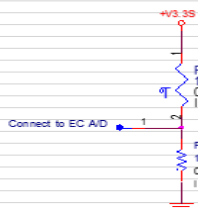
22.2.9 USB 3.0 Disabling and Termination Guidelines
If a USB port(s) are not implemented on the platform, USB signals can be left unconnected. OC pins require a pull-up to V1P8A with 8.2-Kohm to 10-Kohm resistors. When USB OTG feature is not required, USB_OTG_ID and USB_VBUSSENS signals can be left unconnected. Additionally please refer to SPI programming Guide to set the soft strap for disabling USB OTG.
DOC:540602 Ver. 1.2

USB3.0

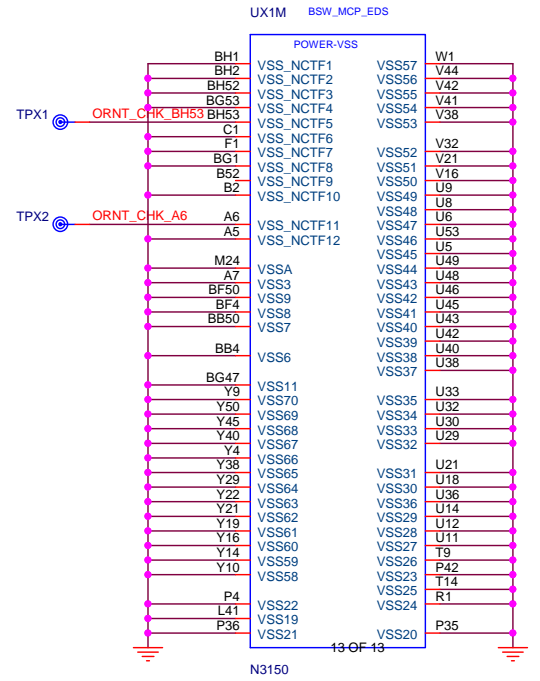
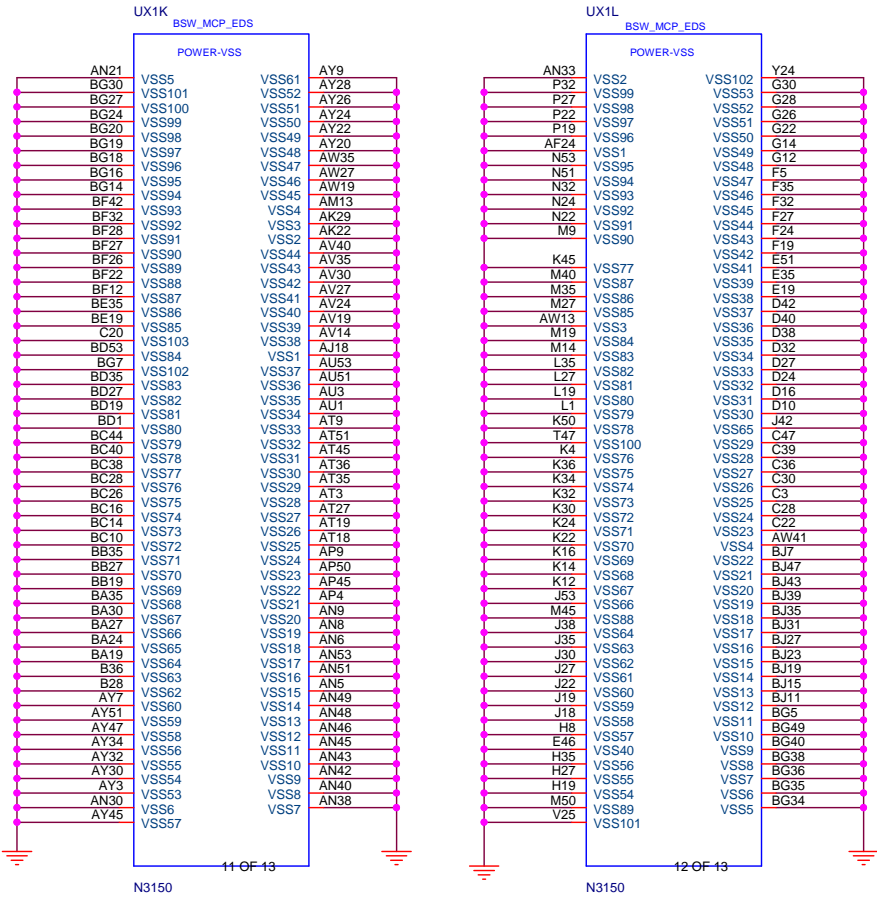
3.7.2 USB 3.0 ports
Leave the unused USB differential signals as NC.
DOC: 544973 Ver. 1.2

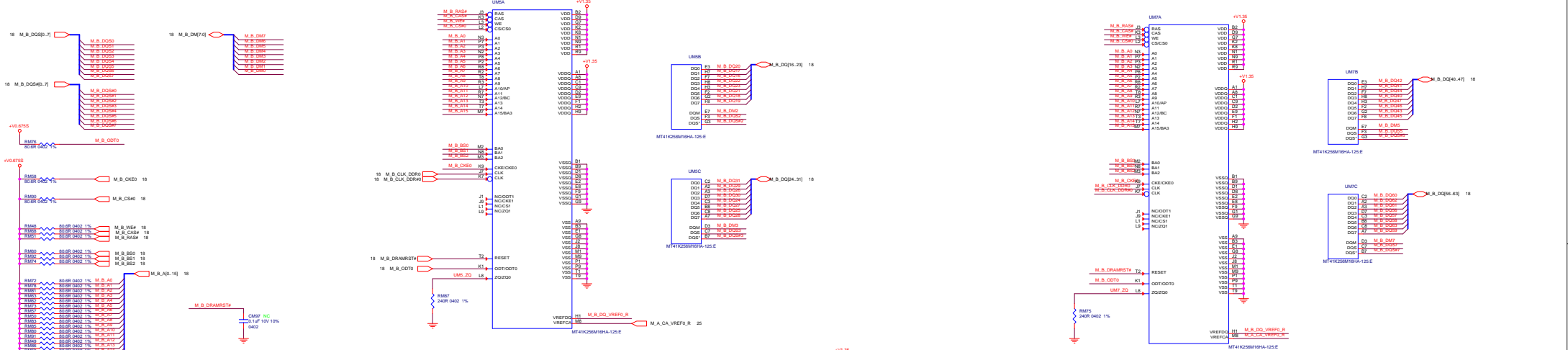


Temperature(°C)	R1(KΩ)	R2(KΩ)	Ym	EC A/D
0	328.09	100	3.3	0.770865292
1	311.72	100	3.3	0.801457195
2	295.31	100	3.3	0.832881487
3	281.73	100	3.3	0.864445590
4	267.94	100	3.3	0.896835513
5	254.94	100	3.3	0.929734603
6	243.63	100	3.3	0.963128079
7	230.93	100	3.3	0.997039294
8	219.95	100	3.3	1.031378924
9	209.53	100	3.3	1.066134244
10	199.67	100	3.3	1.101284832
11	190.32	100	3.3	1.13679424
12	181.42	100	3.3	1.172624547
13	173.04	100	3.3	1.208702659
14	165.08	100	3.3	1.245048104
15	157.42	100	3.3	1.281661090
16	150.32	100	3.3	1.318531256
17	143.51	100	3.3	1.355680480
18	137.04	100	3.3	1.393111589
19	130.91	100	3.3	1.430825634
20	125.08	100	3.3	1.468814537
21	119.55	100	3.3	1.507074471
22	114.28	100	3.3	1.545604108
23	109.28	100	3.3	1.584404598
24	104.52	100	3.3	1.613534129
25	100	100	3.3	1.643
26	95.99	100	3.3	1.683889338
27	91.6	100	3.3	1.724238208
28	87.702	100	3.3	1.758105934
29	83.99	100	3.3	1.793474738
30	80.456	100	3.3	1.828700948
31	77.082	100	3.3	1.864467181
32	73.884	100	3.3	1.897838794
33	70.826	100	3.3	1.931790240
34	67.912	100	3.3	1.965314143
35	65.135	100	3.3	1.998564974
36	62.486	100	3.3	2.030944204
37	59.956	100	3.3	2.063014734
38	57.64	100	3.3	2.094572143
39	55.23	100	3.3	2.125905865
40	53.054	100	3.3	2.156101768
41	50.918	100	3.3	2.185088501
42	48.927	100	3.3	2.213404446
43	47.045	100	3.3	2.24210256
44	45.219	100	3.3	2.272429916
45	43.473	100	3.3	2.300945139
46	41.808	100	3.3	2.327132382
47	40.211	100	3.3	2.353595652
48	38.686	100	3.3	2.379475938
49	37.227	100	3.3	2.404774571
50	35.832	100	3.3	2.4294717

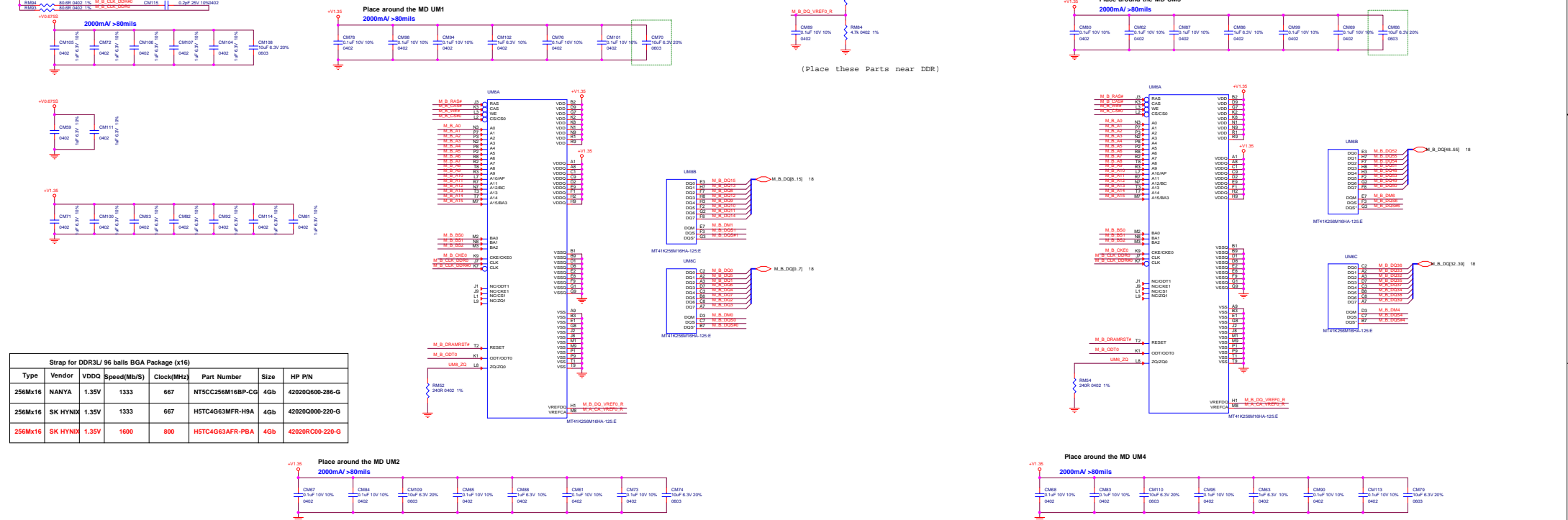


+V3.3A	7,10,13,14,15,16,18,21,27,28,30,32
+V5A	7,10,12,13,14,15,16,28,33
+V3.3S	7,16,19,20,21,23,27,28,29,30,31,34,35
+V3.3AL	8,10,20,21,27,28,29
+V1.8A	7,15,17,19,20,21,23,27,28,29,30,32,34
+V1.8S	7,17,19,20,23,30,34,35





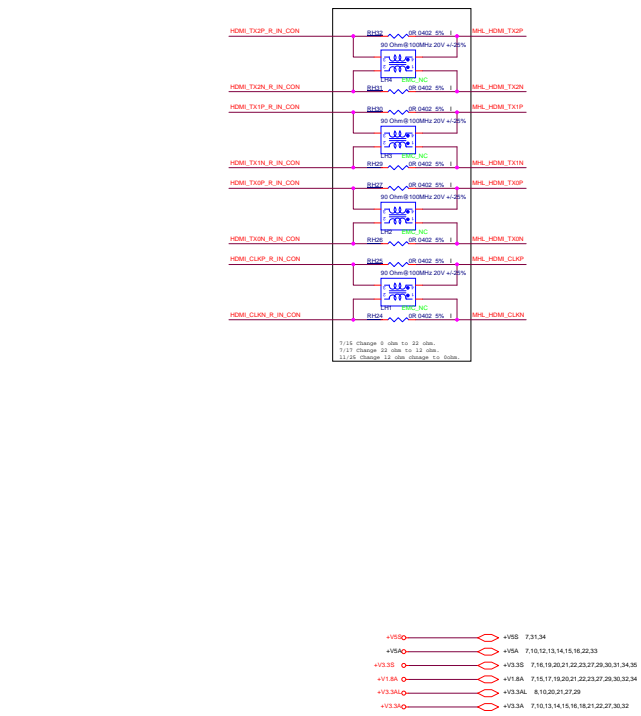
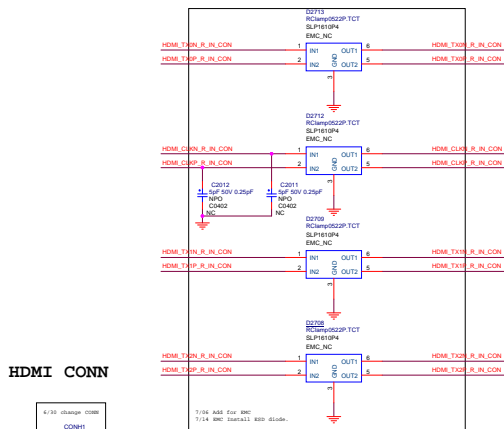
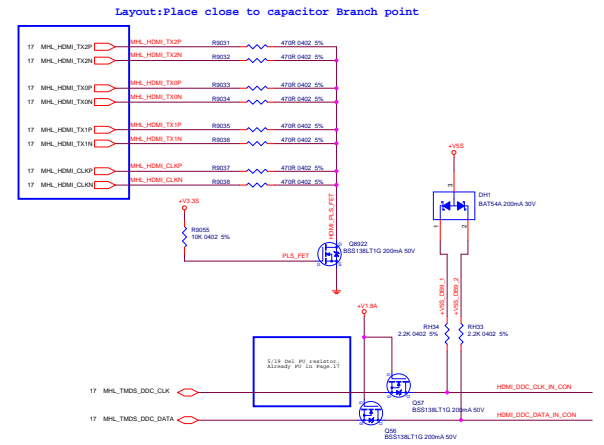
(Place these Parts near DDR)




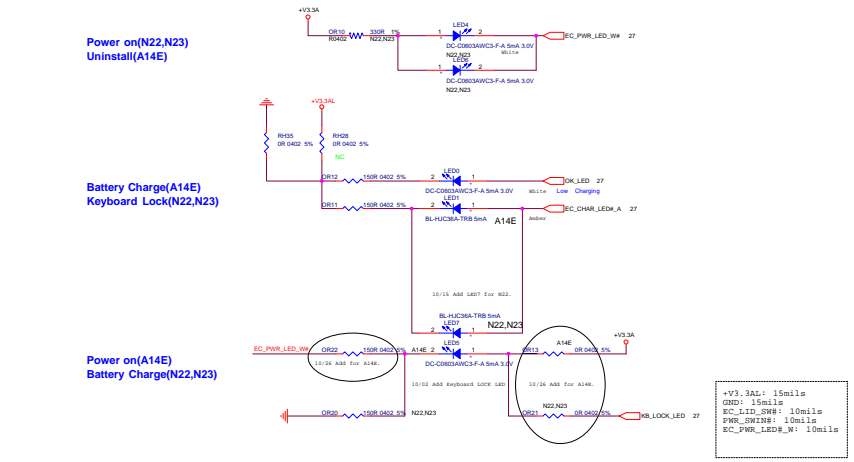
Strap for DDR3L/ 96 balls BGA Package (x16)						
Type	Vendor	VDDQ	Speed(Mb/s)	Clock(MHz)	Part Number	Size
256Mx16	NANYA	1.35V	1333	667	NTSCC256M16BP-CG	4Gb
256Mx16	SK HYNIX	1.35V	1333	667	H5TCA6G3MFR-HBA	4Gb
256Mx16	SK HYNIX	1.35V	1600	800	H5TCA6G3AFR-PBA	4Gb

HDMI Level Shifter

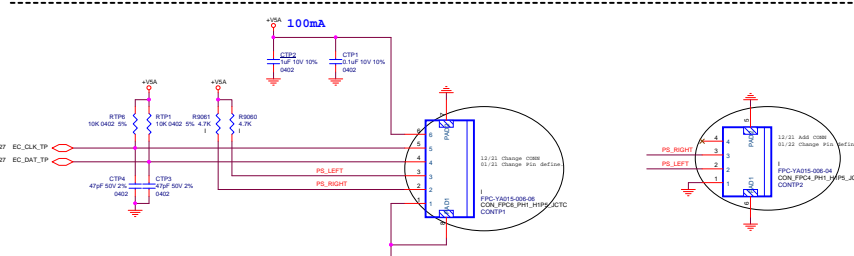
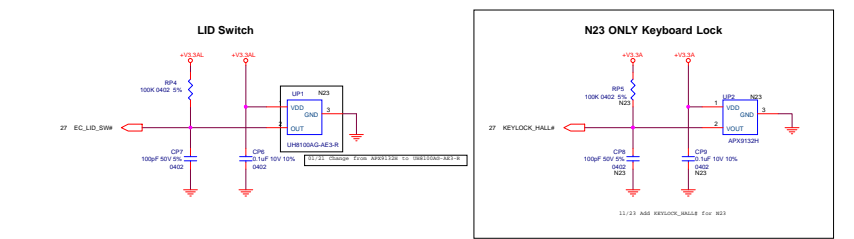
Pin	Name	I/O	Description
12	PDI ¹	I	Chip power down. Active LOW. Internal pull up at +150kΩ, 3.3V I/O PDI ¹ = H: Normal operation (default) L: Chip power down
8	DCIN_EN	I	DC coupling enable; Internal pull down at +150kΩ, 3.3V I/O DCIN_EN = H: AC coupling input (default) L: DC coupling input
13	EQ	I	Receiver equalization setting. Internal pull down at +150kΩ, 3.3V I/O EQ = H: Programmatic EQ for channel loss up to 12.4dB @ 3.0Gbps (default) L: Programmatic EQ for channel loss up to 4.3dB @ 3.0Gbps M: Programmatic EQ for channel loss up to 8.6dB @ 3.0Gbps
16	PRE	I	Output pre-emphasis setting for data; Internal pull down at +150kΩ, 3.3V I/O PRE = H: No pre-emphasis (default) L: 2.5dB pre-emphasis

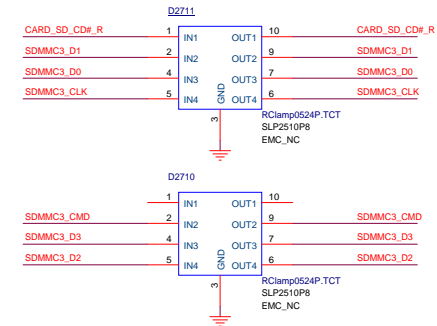


	Project: LENOVO_NB116BT		
	Engineer: Jason		
Size D	Title: PWR LED/LID/TP CONN/HDMI	Rev V01	
Date: Friday, May 06, 2016	Phone: 28	of 38	

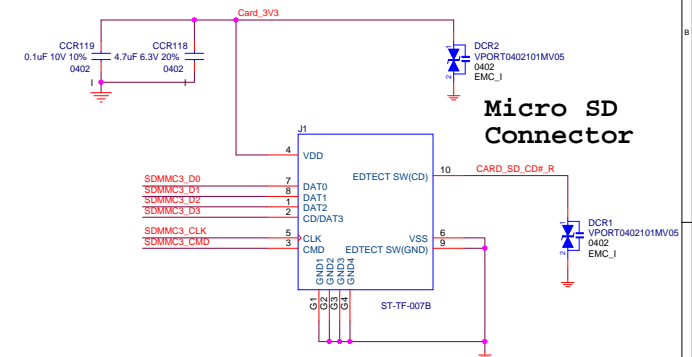


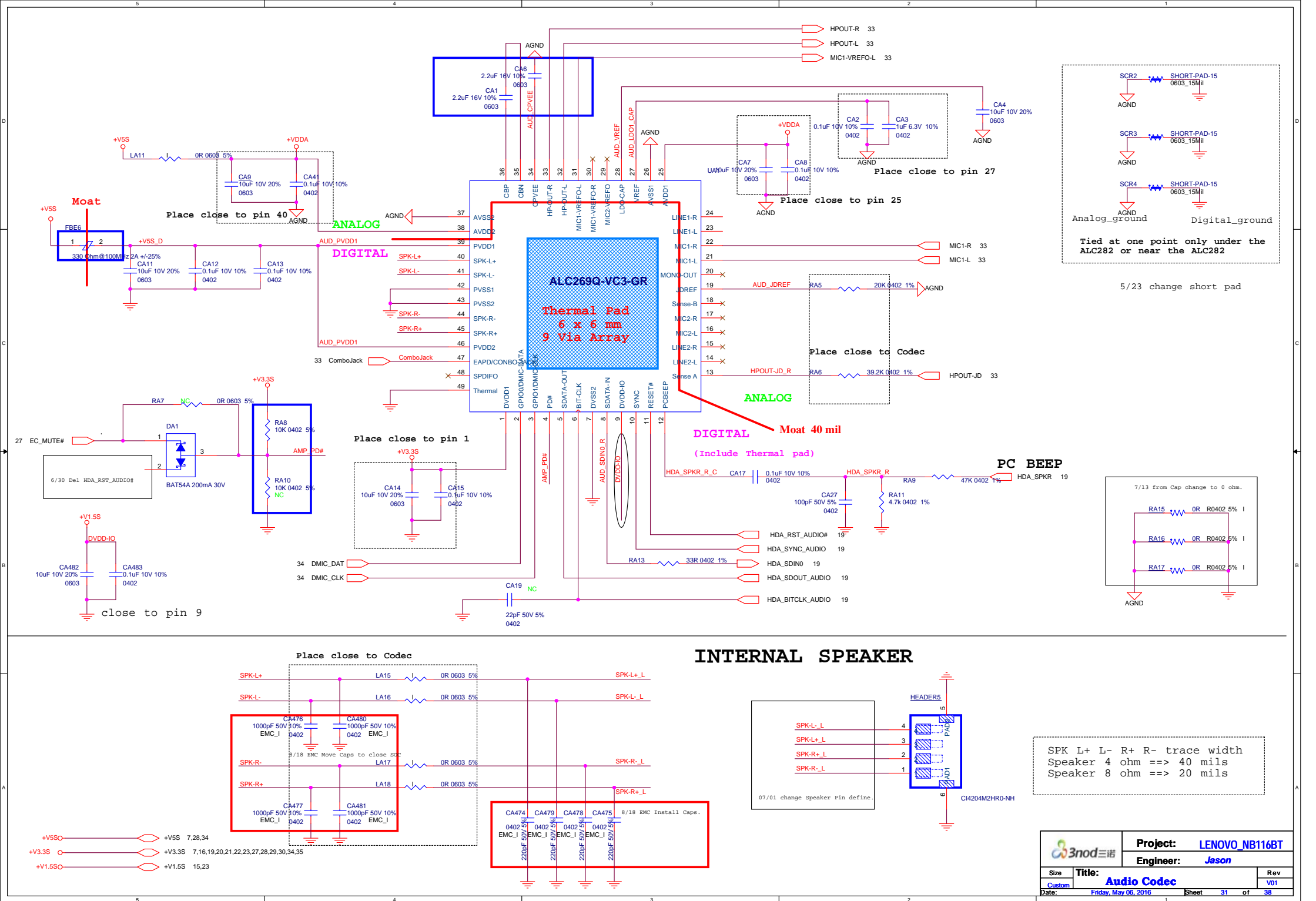
Function	N22	N23	A14E	BOM control	Install	Uninstall
LID	UP1	UP3	UP1	N22	UP1	UP2,UP3,RP5,CP8,CP9
Keyboard Lock	X	UP2	X	N23	UP2,UP3,RP5,CP8,CP9	UP1
				A14E	UP1	UP2,UP3,RP5,CP8,CP9



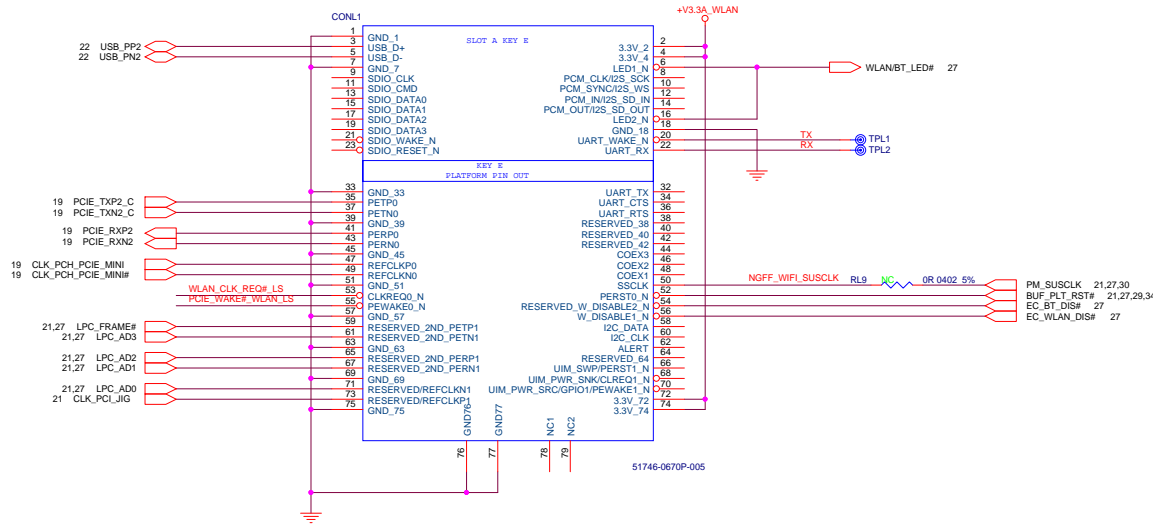
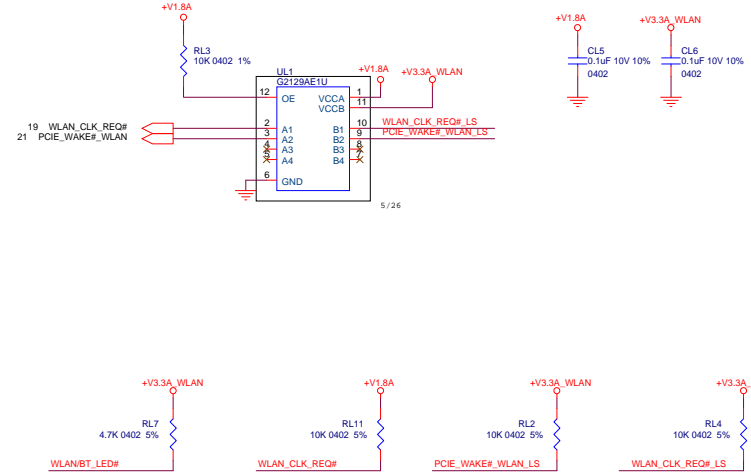
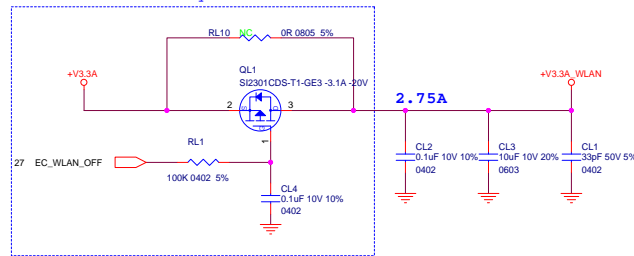


PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2kΩ	75
	7.5kΩ	90
	10.5kΩ	100
	14kΩ	105
	18.7kΩ	110

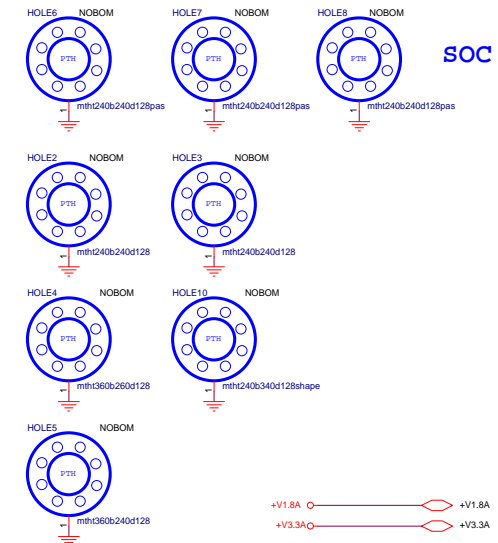




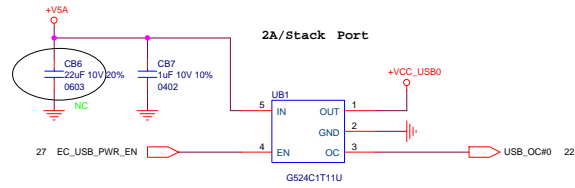
+3_3VAux=>2.75A Peak/1.1A Normal
for connect standby function



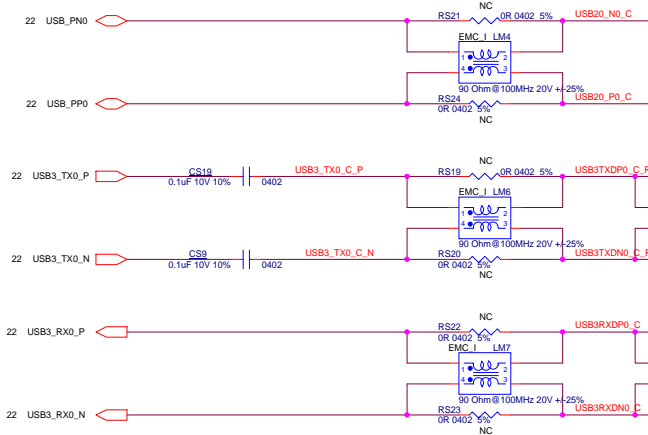
Screw Hole



5/23 CB6 25V 0805 change 10V 0603



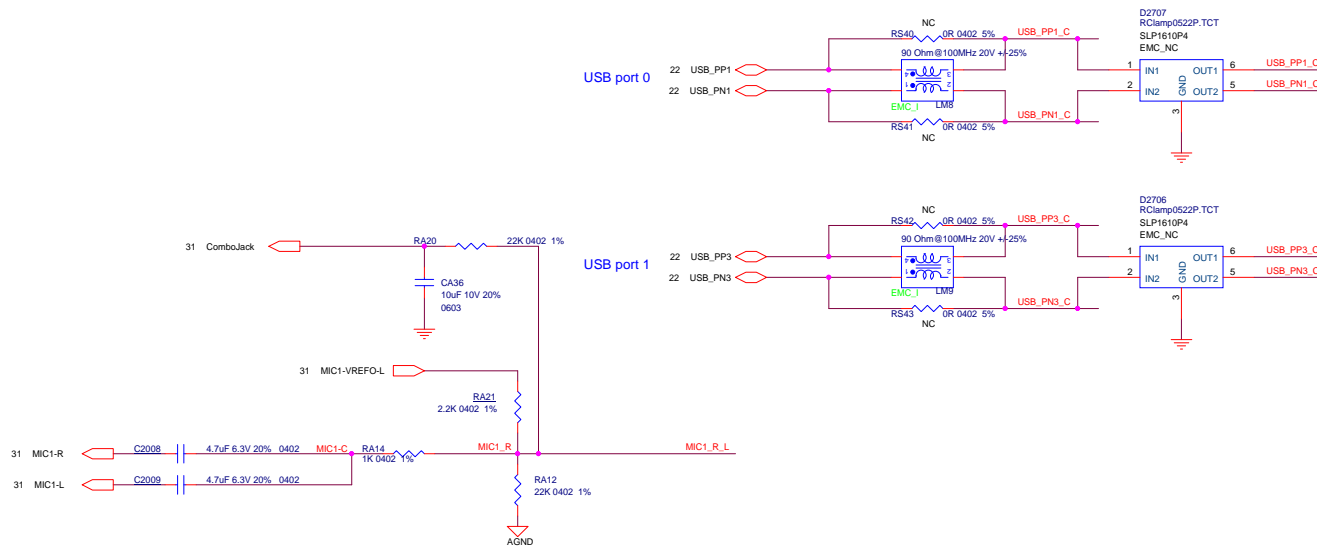
5/23 UB1 change IC



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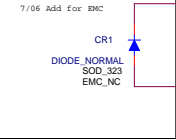
USB port 0

USB port 1

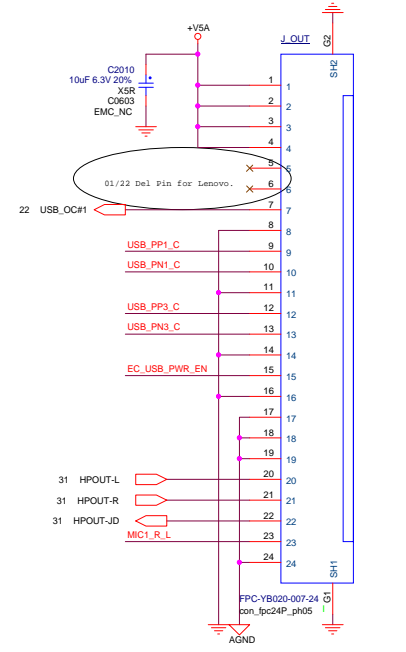
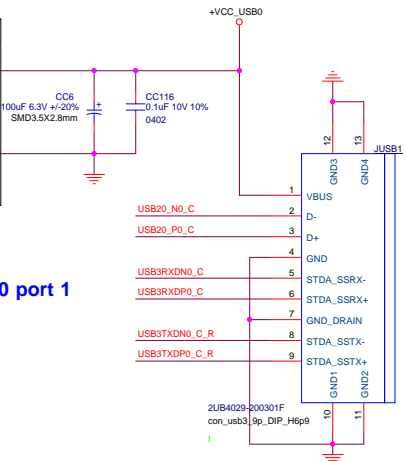


5/18 Remove Charger IC

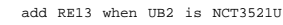
If Install Change to PESD5V0L1BA




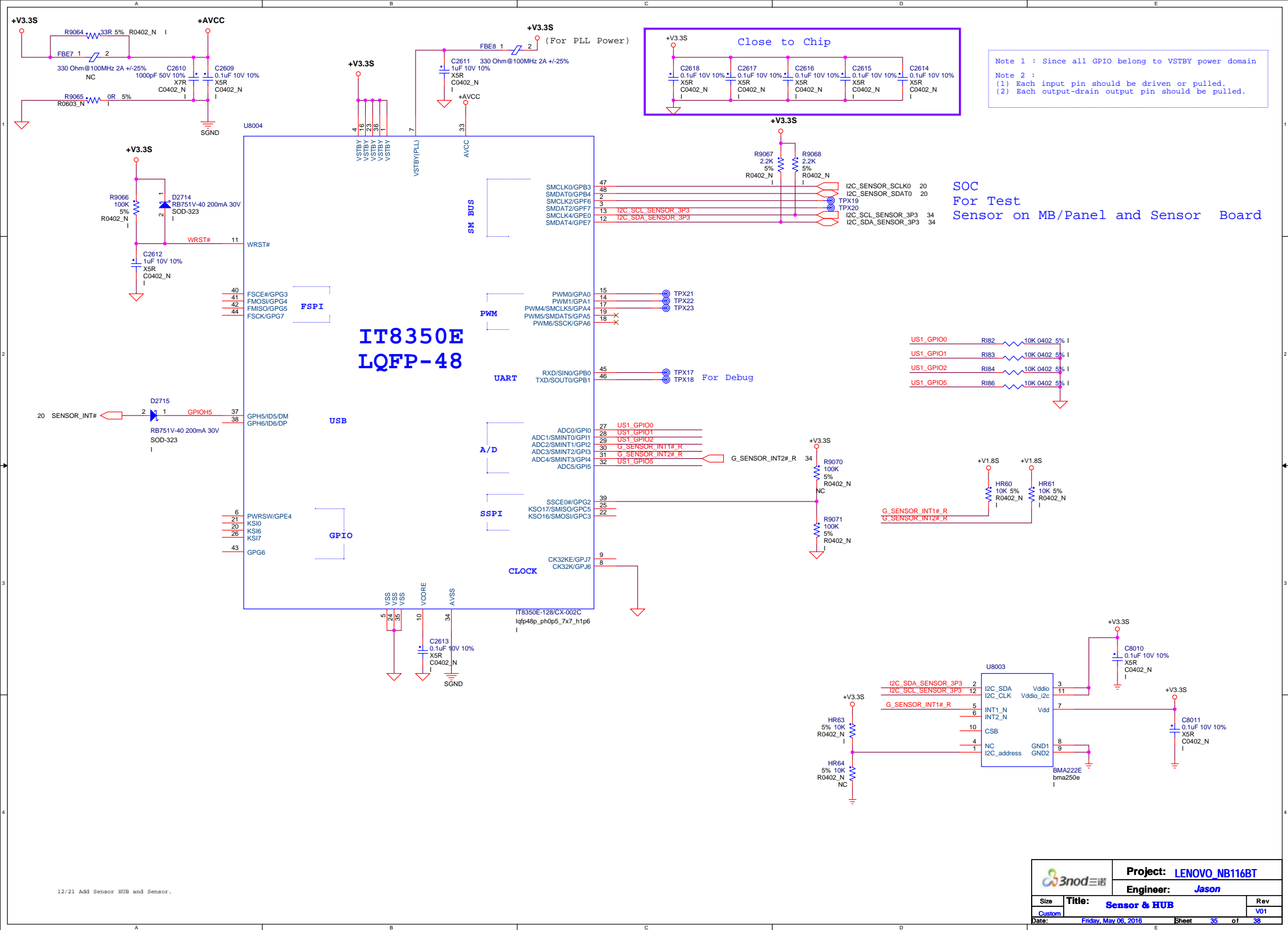
USB2.0/USB3.0 port 1



9/20 add USE NOW



	Project: LENOVO_NB116BT	
	Engineer: Jason	
Size	Title: eDP & CAM	Rev
D		V01



N23

12/15 Page.28 Add CH9 (install) & DCRH1(noninstall) to circuit to solve HDMI hot plug ESD issue.
12/15 Page.34 Add CH10 to solve FBEL issue.

12/21 Page.19 Add QX14,HR66,HR67, Del RX134, for Touch Panel.
12/21 Page.20 Add HR62,HR65,UE3,RE18,RX199,RX200,RX207,RX208,RX209,RX210,RX211,RX212,for Touch Panel and Sensor.
12/21 Page.28 Change CONTP1, Add CONTP2, for new Touch PAD.
12/21 Page.28 Install UP2,RP5,CP8,CP9, for Keyboard LOCK.
12/21 Page.34 Install USB HUB.
12/21 Page.34 Del LK3, Add RK15,RK16,RE19,RE20,QL2,RE17,CE1215 for I2C Touch Panel.
12/21 Page.35 Add Sensor Hub, Sensor.
12/22 Page.27 Change SDMMC3_PWR_EN#_ECI from 28 to 100 pin.
12/24 Page.28 Change Version ID to SIT build, N23.

Already Sent ECN

N23 SIV

01/15 Page.20 Swap SOC_I2C0_CLK,SOC_I2C0_DATA and SOC_I2C5_CLK,SOC_I2C5_DATA
01/19 Page.20 Change UE3 to G2129BAE1U.
01/21 Page.28 Change Touch PAD Pin define.
01/21 Page.28 Change UP1 to UH8100.
01/21 Page.27 Install RI21, for Version SIV.
01/22 Page.28 Change Touch Click Pin define.
01/22 Page.33 Del USB board Pin5.6, for Lenovo suggestion.
01/25 Page.17 Del RX4,RX5,RX6,RX7,RX8,RX9,RX10,RX92,RX11,RX197,RX198,CX108, For change SD solution.
01/25 Page.19 Add CX109,CX110, For change SD solution.
01/25 Page.23 Install RX191, For change SD solution.
01/25 Page.29 Add Card reader controller.
01/27 Page.29 Add UX4 Level shift.
01/29 Page.17 Add RX11.

N23 SIT


03/23 page.19 Add HR68 NC; Add HR69;
03/23 page.34 Add RE22 NC; Add RE21,RE23;
03/23 page.34 DEL CONE1-PIN5;
03/28 page.19 Add RX218 NC; Add RX219; RES HR67 NC;
03/28 page.20 Add RX214,RX215; Add RX216,RX217 ,RX221,RX222 NC; RES RX211,RX212 NC
03/28 page.34 Add RX220; RES RE20 NC; Add RX223 NC

N23 SVT

05/06 page.34 Add RE24;
05/06 page.34 NC QL2,RE17,CE1215;

EMC

11/20 Page.16 Add reserve EMC plane Caps.
11/20 Page.33 Install LM8,LM9.

		Project: LENOVO_NB116BT	
		Engineer: Jason	
Size	Title: Change List		Rev
Custom			V01
Date: Friday, May 06, 2016		Sheet	37 of 38

POWER CHANGE LIST

9/2	Page.8	Change battery connector CN0802 Change CN0802 pin definition. Pin3 BATT+ ==> CLK. Pin5 SMC ==> TS(ID) Pin6 TH ==> NA Pin9 BATT- Delete Delete R0806,R0807,C0805,R0808,C0807 Add R0831,R0832 100R
9/2	Page.8	Remove shipping mode circuit. Delete R0830,C0821,R0826,R0825,Q0801,Q0802,R0827,R0828,C0822.
9/2	Page.8	Remove Gauge IC circuit Delete U0801,R0836,R0833,R0834,C0827,C0825,C0826,R0824,R0823,R0835,R0839,R0838,C0808,C0819,C0820,C0823,R0822,R0829,R0837,C0824